Evaluation of Ultrahigh-Speed Magnetic Memories Using Field-Free Spin–Orbit Torque

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Ultrahigh-speed magnetization switching mechanism is strongly pursued, as it can improve the write performance of the magnetic random access memory (MRAM) and further extend the application area of spintronics. Currently, a well-studied switching mechanism is the spin transfer torque (STT), whose speed, however, is limited by an intrinsic incubation delay. Recently, spin–orbit torque (SOT) was proposed to solve the speed bottleneck of the STT. In this paper, we evaluate the potential of two types of SOT-MRAMs, whose data can be ultrafast written based on the recently discovered field-free SOT mechanisms, respectively. A cross-layer analysis is presented involving device modeling, circuit-level optimization, and architecture-level evaluation. First, the principle of the magnetization switching is analyzed with the macrospin simulation. Then, the optimization strategies at the circuit level are generalized through the SPICE-type simulation. Finally, we build up the memory architecture with the SOT-MRAMs, STT-MRAM, and static RAM. Their read/write performances are evaluated with NVSim software. It is demonstrated that one of the studied SOT-MRAMs shows the promising prospect in the non-volatile memory, especially suitable for high-capacity cache.

***Index Terms*— Cross-layer analysis, magnetic random access memory (MRAM), spin–orbit torque (SOT), ultrahigh-speed magnetization switching.**

I. Introduction

NON-VOLATILE memories (NVMs) have been intensively investigated by both the academia and industry for solving the issue of soaring static power caused by the scaling of transistors. In the general memory architecture, main memory (e.g., dynamic random access memory), and cache [e.g., static random access memory (SRAM)] are considered as the key modules influencing the system performance, since they bridge the gap between the processor and hard disk drive or solid state drive. For the main memory, high-density integration and large capacity storage are the concerning advantages since the numerous running programs are loaded inside it. While for the cache, high-access speed is pursued as the data are frequently and directly transferred between the cache and processor. However, currently the operation speed of mainstream NVMs varies from several nanoseconds to hundreds of nanoseconds [1], which cannot meet the requirement of non-volatile cache.

Recently, sub-nanosecond magnetization switching was demonstrated with an emerging mechanism called spin–orbit torque (SOT) [2]–[6], which qualifies the magnetic RAM (MRAM) for the non-volatile cache. The memory cell of the MRAM is magnetic tunnel junction (MTJ), which, according to the direction of the easy axis, can be classified into two types: perpendicular-anisotropy MTJ (p-MTJ) and in-plane-anisotropy MTJ (i-MTJ). However, some issues need to be overcome before either p-SOT-MTJ or i-SOT-MTJ is applied to the cache. For the p-MTJ, the easy axis is vertical to the polarization direction of the SOT-induced spin current. Thus, an additional magnetic field is required to break this symmetry and achieve the deterministic switching, impeding the practical realization of the related circuits and systems. For the i-MTJ, the easy axis is aligned to the SOT-induced spin polarization. Thus, the deterministic switching can be implemented without the need of the magnetic field. However, the incubation delay of the spin torque is not eliminated, resulting in an unsatisfying switching speed.

In this paper, we investigate two types of recently discovered SOT-based mechanisms [7], [8], which can induce ultrafast field-free magnetization switching in the p-MTJ and i-MTJ, respectively. Thus, the above-mentioned issues are solved. The goal of this paper is to evaluate the application potential of the SOT-MRAMs based on these two switching mechanisms. We present our works at the device-, circuit-, and architecture-levels in Sections II–IV, respectively. Finally, the conclusion is drawn in Section V.

II. Device Model

A. Device Structure

The SOT-MTJs studied in this paper are illustrated in Fig. 1(a) and (b), where the p-MTJ or i-MTJ is fabricated above a heavy metal with strong spin–orbit coupling. The free layer of the MTJ is contacted to the heavy metal. A charge current passing the heavy metal induces the SOT (including dampinglike torque and fieldlike torque) through the spin Hall

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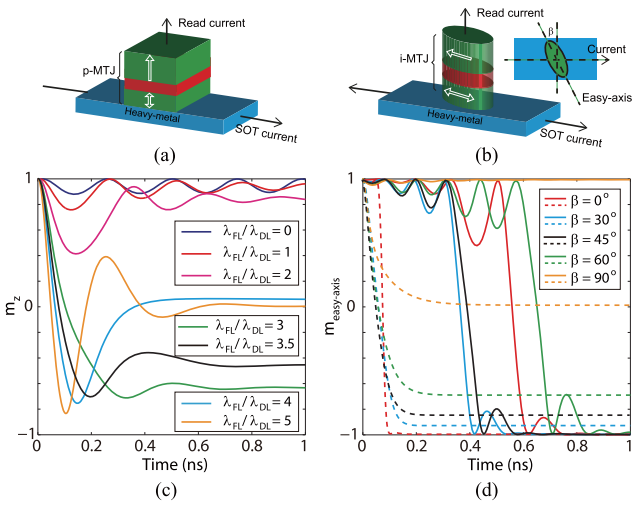

Fig. 1. (a) and (b) Schematic of p-SOT-MTJ and i-SOT-MTJ studied in this paper. (c) Macrospin simulation results of the time-dependent z-component magnetization (m_z) in the p-SOT-MTJ. The SOT current density is set to $4\times 10^{11} A/m^2$. (d) Macrospin simulation results of the time-dependent easy-axis-component magnetization ($m_{\text{easy}-\text{axis}}$) in the i-SOT-MTJ. The SOT current densities are $10\times 10^{11} A/m^2$ (solide lines) and $50\times 10^{11} A/m^2$ (dashed lines). The other parameters are configured as Table I.

effect or Rashba effect. The magnetization dynamics of the free layer can be described by a modified Landau–Lifshitz–Gilbert (LLG) equation, as

$$\frac{\partial \mathbf{m}}{\partial t} = -\gamma\,\mu_0 \mathbf{m}\times\mathbf{H}_{\text{eff}} + \alpha\mathbf{m}\times\frac{\partial \mathbf{m}}{\partial t} - \lambda_{\text{DL}}\xi J\mathbf{m}\times(\mathbf{m}\times\boldsymbol{\sigma}) - \lambda_{\text{FL}}\xi J\mathbf{m}\times\boldsymbol{\sigma} \quad (1)$$

where $\mathbf{m}$ is the unit vector of the free-layer magnetization, $\mathbf{H}_{\text{eff}}$ is the effective field, and $\boldsymbol{\sigma}$ is the unit vector of the SOT-induced spin polarization. γ is the gyromagnetic ratio. μ_0 is the vacuum permeability. α is the damping constant. J is the SOT current density. ξ is a device-dependent parameter. λ_{DL} and λ_{FL} represent the strengths of the dampinglike and fieldlike torques, respectively.

B. Mechanisms of the Magnetization Switching

Two SOT-based mechanisms were recently demonstrated to implement the ultrafast field-free switching of the p-MTJ and i-MTJ, respectively. They are described as follows. For the p-MTJ, if $\lambda_{\text{FL}}/\lambda_{\text{DL}}$ is set to be large enough and in an appropriate range, the magnetization can be switched at sub-nanosecond speed [7]. For the i-MTJ, by tilting the easy axis from the direction of the SOT-induced spin polarization, the SOT is enhanced to decrease the incubation delay and accelerate the magnetization switching [8]. Fig. 1(c) and (d) shows the macrospin simulation results of the above-mentioned switching mechanisms, respectively. They are in good agreement with the above-mentioned analysis.

It is important to mention that the switching is not bipolar in Fig. 1(c). Take $\lambda_{\text{FL}}/\lambda_{\text{DL}} = 3$, for example, the magnetization is always switched to the opposite state once an SOT current with appropriate amplitude is applied, regardless of the current polarity. Thereby, a read-before-write operation is required by the practical realization of the related MRAM.

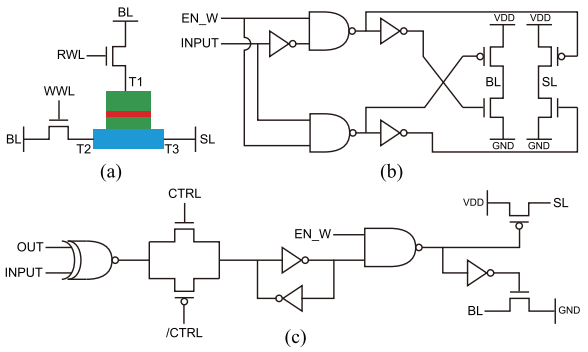

Fig. 2. (a) Bit-cell structure of the SOT-MRAM. Write drivers for (b) i-SOT-MRAM and (c) p-SOT-MRAM.

In addition, note that an excessively large $\lambda_{\text{FL}}/\lambda_{\text{DL}}$ drives the magnetization to be in-plane, which is a metastable position for the magnetization switching. To achieve the reliable switching, the SOT current density needs to be properly decreased in the case of stronger fieldlike torque.

It is seen from Fig. 1(d) that the trajectories of magnetization switching are significantly influenced by the magnitudes of both the tilting angle β and SOT current density. First, the switching speed can be optimized by adjusting the tilting angle β. Second, once the SOT current density is sufficiently large, the incubation delay is almost eliminated [see dashed lines in Fig. 1(d)]. For $\beta = 90°$, the magnetization is rotated to hard axis. In this case, an out-of-plane magnetic field is required to break the symmetry and achieve the deterministic switching. For the other cases, the deterministic bipolar switching occurs due to the breaking of the symmetry.

Using *Verilog-A* language, we have developed two electrical models for two types of SOT-MTJs described earlier. The magnetization dynamics are resolved based on LLG equation [see (1)]. The MTJ resistance is calculated by considering the Brinkman model, bias-dependent tunneling magnetoresistance, and Slonczewski's theory [9]. Single-cell simulation has been performed to validate the functionality of the electrical models.

III. Circuit-Level Optimization

A. Circuit Design

Using the developed electrical models and CMOS 28 nm design kit, we design two SOT-MRAMs based on the two switching mechanisms described in Section II-B. In the following, these two SOT-MRAMs are specifically referred to with terms "p-SOT-MRAM" and "i-SOT-MRAM," respectively, unless otherwise stated. The bit-cell structure of the MRAMs is shown in Fig. 2(a), where two access transistors are associated with an SOT-MTJ to form a 2T1J bit cell. The read operation is performed with a pre-charge sensing amplifier [10], [11]. The write drivers for these two SOT-MRAMs are illustrated in Fig. 2(b) and (c), respectively. The i-SOT-MRAM uses the write driver shown in Fig. 2(b), where the bi-directional current is generated by controlling the pull-up and pull-down transistors. The direction of the current depends on the state of "INPUT."

TABLE I
PARAMETERS FOR DEVICE AND CIRCUIT

Parameter	Value
MTJ area	40 nm × 40 nm (p-MTJ) 60 nm × 120 nm × $\pi/4$ (i-MTJ)
Heavy-metal dimension	40 nm × 60 nm × 2 nm (p-MTJ) 120 nm × 140 nm × 2 nm (i-MTJ)
Free layer thickness	1 nm (p-MTJ); 2 nm (i-MTJ)
Damping constant	0.02
Spin Hall angle	0.3
Effective anisotropy field for p-MTJ	1.33×10^5 A/m
In-plane anisotropy field for i-MTJ	1.87×10^4 A/m
Saturation magnetization	1×10^6 A/m
R. A. of the MTJ	$10\ \Omega \cdot \mu m^2$
TMR	120%
Heavy-metal resistivity	$200\ \mu\Omega \cdot$ cm
Power supply	1.1 V

For the p-SOT-MRAM, a read-before-write operation is required, as mentioned above in Section II-B. Therefore, we employ a XNOR gate to compare the data stored into the bit cell ("OUT") with the data to be written ("INPUT"), as shown in Fig. 2(c). The comparison result is passed into a latch through a transmission gate. As a result, the write current is applied to the bit cell if and only if the state of "INPUT" is different from that of "OUT". In addition, as the written data are independent on the direction of the write current (as explained in Section II-B), only two driving transistors are needed to provide a unidirectional current.

B. Results and Discussions

The read/write operation of the above-mentioned SOT-MRAMs has been validated through the transient simulation, as shown in Fig. 3. The parameters are configured as Table I that reflects the typical technologies for i-MTJ and p-MTJ. Fig. 4 shows the results of access transistor size and write energy. Here, the write latency is fixed to 0.4 ns, which meets the speed requirement of the cache.

For the p-SOT-MRAM, the access transistors are shrunk as the fieldlike torque is enhanced. It means that the required write current is decreased since more efficient fieldlike torque promotes the precession of the magnetic moments. It is worth noting that the write current is not allowed to be arbitrarily increased. Excessively,a large current induces too strong SOT, including dampinglike torque $\lambda_{\mathrm{DL}}\xi J\mathbf{m}\times(\mathbf{m}\times\boldsymbol{\sigma})$ and fieldlike torque $\lambda_{\mathrm{FL}}\xi J\mathbf{m}\times\boldsymbol{\sigma}$. Both of them suppress the other torques and tend to drive the magnetization along the direction of $\boldsymbol{\sigma}$ (in-plane direction). In this situation, the magnetization relaxes toward $+z$- or $-z$-axis with the equal probability after the current is OFF. Thereby, the deterministic switching cannot be achieved [7].

Similarly, the write energy of the p-SOT-MRAM decreases with the increasing $\lambda_{\mathrm{FL}}/\lambda_{\mathrm{DL}}$. This is mainly attributed to the decrease of the write current. But an exception occurs while $\lambda_{\mathrm{FL}}/\lambda_{\mathrm{DL}}$ increases from 3.5 to 4.0. The possible reason is

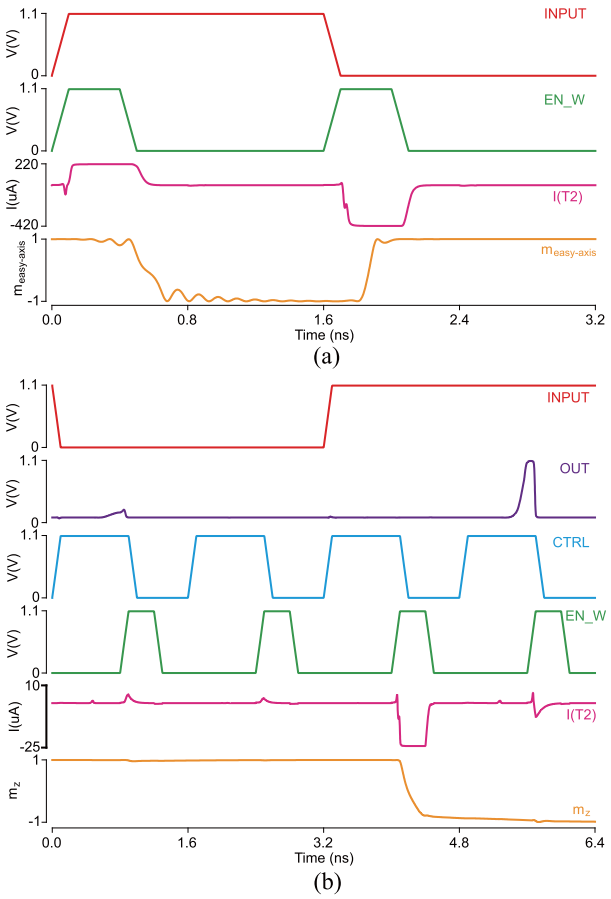

Fig. 3. Transient simulation of (a) i-SOT-MRAM and (b) p-SOT-MRAM.

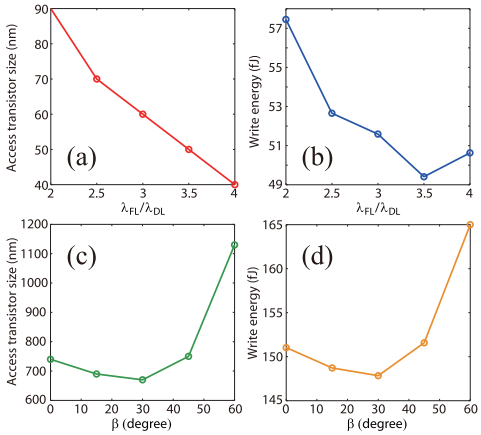

Fig. 4. Simulation results of the access transistor size and write energy. (a) and (b) p-SOT-MRAM. (c) and (d) i-SOT-MRAM.

that the transient impulse consumes more energy during the rising/falling edges of pulses.

For the i-SOT-MRAM, the optimal performance is obtained by setting the tilting angle β to a specific value (30° in Fig. 4). These results may be explained as follows. In the case of smaller β, the dampinglike torque $(\mathbf{m}\times\boldsymbol{\sigma}\times\mathbf{m})$ becomes stronger with the increasing β. Correspondingly, both the write current and energy are decreased. However, too large β causes more processions around the easy axis, although the initial

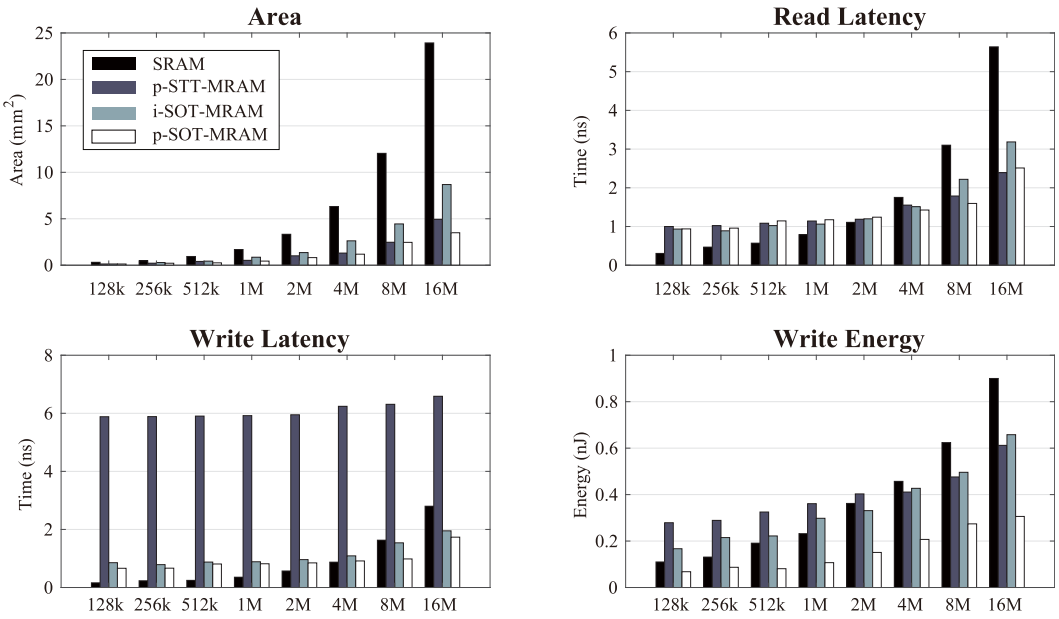

Fig. 5. Memory architecture-level results evaluated by *NVSim*, indicating the comparison among various MRAMs at different capacities.

dampinglike torque is enhanced. As a result, the performance of magnetization switching is degraded in the case of large β.

From Fig. 4, it is inferred that the p-SOT-MRAM significantly outperforms the i-SOT-MRAM. This can be explained by at least three reasons. First, the size of the i-MTJ has to be larger than that of the p-MTJ to maintain the satisfactory shape anisotropy, which means that a wider heavy metal and a higher write current. Second, the incubation delay can be fully eliminated by the huge fieldlike torque in the p-SOT-MRAM. In contrast, there is still precession happening during the magnetization switching of the i-SOT-MRAM. Third, the write current of the p-SOT-MRAM is unidirectional; thus, the source degeneration issue of the access transistor is avoided [6].

IV. Memory Architecture-Level Evaluation

Based on the circuit-level analysis, we evaluate the performance of the memory architecture with *NVSim* [12]. The comparison of the performance among the conventional SRAM, spin transfer torque (STT)-MRAM, and the presented SOT-MRAMs is provided. The optimal results of Fig. 4(c) and (d) are used as the configuration parameters of the i-SOT-MRAM (i.e., $\beta = 30°$). Considering that the allowed minimum width of the transistor is 80 nm, we choose the result of $\lambda_{\mathrm{FL}}/\lambda_{\mathrm{DL}} = 2$ in Fig. 4(a) and (b) for the p-SOT-MRAM. The device-level parameters of the STT-MTJ (size, damping constant, anisotropy field, and so on.) are set to be the same as those of the p-SOT-MTJ. The circuit-level parameters of the STT-MRAM are obtained through the *Spectre* simulation. The results of the SRAM are provided by *NVSim* based on the default settings. The comparative results are shown in Fig. 5.

As it can be seen, the area of the MRAMs is comparable to that of the SRAM in the case of low capacity. However, with the increasing capacity, the area is dominated by the size of bit cell rather than peripheral circuits. As a result, the SRAM occupies much larger area than the MRAMs, since the MRAM bit cell is smaller than six-transistor SRAM cell. Among the various MRAMs, i-SOT-MRAM induces the largest area overhead due to the large-size access transistors.

Concerning the read latency, there is almost no difference among the various MRAMs if the capacity is not too large. However, the i-SOT-MRAM needs longer read latency when the capacity is higher, since the parasitic capacitances of the large transistors become more significant. The same reason can explain the results of the SRAM.

The STT-MRAM takes the longest write latency, as the intrinsic incubation delay of the STT mechanism deteriorates the speed of the magnetization switching. The SRAM requires shorter write latency compared with the SOT-MRAMs in the case of low capacity. However, the interconnection delay becomes more significant as the capacity is enlarged; thus, the write latency of the SRAM increases more quickly than that of the SOT-MRAMs.

The p-SOT-MRAM consumes the lowest write energy thanks to the low-write current and short write latency. For the i-SOT-MRAM and STT-MRAM, the difference of their write energies is not as large as that of their write latencies, since the i-SOT-MRAM carries larger write current due to the larger device size. Similar to the above-mentioned results, the write energy of the SRAM soars with the enlarging capacity.

In sum, the SRAM is a good candidate for the low-capacity cache. However, the p-SOT-MRAM shows better performance while it is used to construct high-capacity non-volatile cache.

V. Conclusion

Through the cross-layer analysis, we have studied two SOT-MRAMs whose data are written by two recently discovered switching mechanisms, respectively. Macrospin simulation demonstrated that ultrafast field-free magnetization switching

can be achieved with these two mechanisms. Then, the circuit-level simulation indicated that the performance of the studied SOT-MRAMs can be optimized by adjusting the device parameters. Finally, based on the memory architecture-level evaluation, we pointed out that one of the studied SOT-MRAMs promises to replace the SRAM in the application of the high-capacity cache.

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