A novel circuit design of true random number generator using magnetic tunnel junction

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ABSTRACT

Random numbers are widely used in the cryptography and security systems. However, most of the true random number generators (TRNG) which use physical randomness are with high complexity and high power consumption. This paper proposes a new TRNG circuit using magnetic tunnel junction (MTJ). As one of the reliability issues in MTJ based circuit, the stochastic switching behavior provides a perfect physical source of randomness. The functionality of proposed design is validated by transient simulations with 28nm fully depleted silicon-on-insulator (FDSOI) technology and an accurate MTJ compact model. Simulation results show that our design can generate accurate random bitstream stably. The reliability analysis concerning process variation of MTJs and transistors proves the good variability tolerance of our TRNG design. Furthermore, our design can output stable random bitstream around 30 tuning steps.

CCS Concepts

•Hardware → Integrated circuits; Spintronics and magnetic technologies; •Security and privacy → *Security in hardware;*

Keywords

true random number generator, FDSOI, magnetic tunnel junction, stochastic switching, process variation

1. INTRODUCTION

Random numbers are always necessary in many traditional areas, e.g., Monte Carlo simulations, cryptography, statistical sampling and many other security applications [1, 2]. Moreover, with the rapid development of digital ecosystems, random numbers are essential for the security of online transactions and mobile applications. Thus, algorithms with fast speed, low power and high reliability are required to design true random number generators (TRNG). Physical randomness is usually used as entropy sources in conventional TRNG, such as thermal noise, metastability, and oscillator jitter [3]. However, these TRNGs all require extensive post-processing to guarantee a high level of random output, which degrades the performance in terms of speed, power, and area [4]. Consequently, it is urgent to explore new methods of generating random numbers for low complexity design, compact area, high randomness, and reliable operation.

The stochastic behavior of emerging non-volatile devices have been considered as a promising physical noise source for TRNGs [5, 6]. With the rapid development of non-volatile devices, many novel TRNG designs have been proposed by using spin dice [7], memristor [8], and magnetic tunnel junction (MTJ) [9–12]. Compared with the conventional CMOS based TRNGs, the magnetic devices based technology designs can effectively achieve simplified structure, more compact area, higher speed and better energy-efficiency. However, the process variations of MTJ and transistors have not been taken into account in these designs, thus the robustness remains doubtful. As the exact probability is critical for TRNG, it is essential to guarantee its variability awareness.

This paper describes our recent work of a new TRNG circuit design. The feasibility of the proposed solution is verified by using 28nm ultra thin body and buried oxide fully depleted silicon-on-insulator (UTBB FD-SOI) technology and a compact model of MTJ. This model includes reliability issues of process variations, stochastic switching, temperature fluctuation and dielectric breakdown phenomenon [13]. It has been integrated in the design of hybrid MTJ/FDSOI circuits and systems to analyze and optimize operation speed, area and energy performance [14]. Compared with conventional bulk CMOS, FDSOI technology is very promising in power efficiency, scalability and cost [15, 16].

The rest of the paper is organized as follows. Section 2 introduces physical mechanism behind stochastic switching behavior of PMA-MTJ. In Section 3, the compact model which includes stochastic switching is presented in details. Section 4 focuses on the circuit design of TRNG. Section 5 validates the design by performing transient simulation and gives some comparison with other work, followed by the conclusion.

2. STOCHASTIC SWITCHING

Recently, MTJ switched by Spin Transfer Torque (STT) has attracted much attention in research community owing to its great potential in the next generation of non-volatile

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memories. Compared with conventional memories, STT-MTJ based magnetic random-access memory (MRAM) features high power efficiency, fast speed operation, infinite endurance, high density and compatibility with standard CMOS process [17]. Moreover, MTJ with perpendicular magnetic anisotropy (PMA) behaves better performance in terms of thermal stability, critical current and access speed compared to that with in-plane magnetic anisotropy [18]. Figure 1 shows the typical structure of STT-PMA-MTJ. MTJ consists of three layers: two ferromagnetic (FM) layers separated by an insulating oxide barrier. The nanopillar resistance (R_p, R_{ap}) depends on the relative magnetization of the two FM layers (Parallel (P) or Anti-Parallel (AP)). The resistance difference is characterized by Tunnel Magnetoresistance Ratio TMR = $(R_{ap}$-$R_p)/R_p$. With STT mechanism, MTJ changes between two states when a bidirectional current I is higher than the critical current I_{c0}.

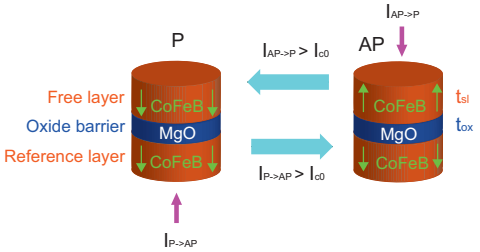

Figure 1: Typical structure of PMA-MTJ.

Despite excellent potential in STT-MTJ, the switching of MTJ has been revealed intrinsically stochastic due to thermal fluctuation of magnetization [19, 20]. As a result, the switching delay of MTJ is not a deterministic value but follows a statistical distribution. Because of this phenomenon, write errors might occur with insufficient writing current or short writing pulse, while unexpected switching may happen in sensing operation [21]. Nonetheless, this property can be appropriately utilized as a randomness source for TRNG circuit implementation.

It has been well confirmed, both theoretically and experimentally that a spin-polarized current will deposit its spin-angular momentum into the magnetic system when passing through a small magnetic conductor. Consequently, it causes the magnetic moment to precess or even switch when the spin-current is sufficient [22]. Figure 2 illustrates the precession of magnetization under the influence of a spin current. Due to the thermal fluctuation of magnetization, the initial state of free layer magnetic moment (represented by θ) is different at each measurement. This leads to the stochastic reversal of free layer magnetization, which is revealed by the random duration for the resistance reversal (see Figure 3).

3. COMPACT MODELING OF STOCHASTIC SWITCHING

The electrical behaviors of PMA-MTJ devices have been integrated in the compact model of previous work [23]. The static behavior is composed of calculating the resistance and critical switching current I_{c0} [18, 24]:

$$R_p = \frac{t_{ox}}{(F \cdot \bar{\varphi}^{1/2} \cdot Area)} \cdot exp(coef \cdot t_{ox} \cdot \bar{\varphi}^{1/2}) \qquad (1)$$

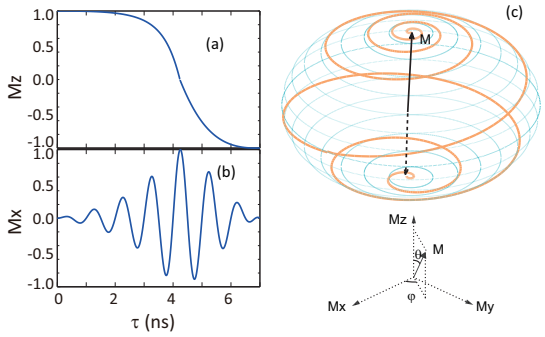

Figure 2: The precession of magnetization under the influence of a spin current: Time dependence of (a) Mz and (b) Mx, (c) The reversal process of magnetic moment.

where $\bar{\varphi}$ is the average potential barrier height of MgO, coef=$1.025nm^{-1}eV^{-1/2}$ is a fitting parameter and F is corresponding to RA product [24].

$$I_{c0} = \alpha \frac{\gamma e}{\mu_B g}(\mu_0 M_s) H_k V_{sl} \qquad (2)$$

$$\Phi_b = \frac{\mu_0 M_s H_k V_{sl}}{2} \qquad (3)$$

where Φ_b is the barrier energy, H_k is the effective anisotropy field, μ_0 is permeability of free space, M_s is the saturation magnetization, α is the magnetic damping constant, γ is the gyromagnetic ratio, e is the elementary charge, μ_B is the Bohr magneton, V_{sl} is the volume of the free layer, g is the spin polarization efficiency factor.

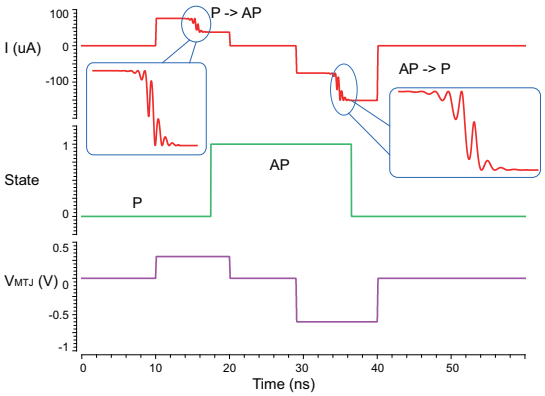

Figure 3: The transition of electrical parameters during the switching process of MTJ under voltage pulses. The oscillation is induced by the precessional motion of perpendicular anisotropy filed.

The dynamic model is mainly composed of calculating the average switching delay τ_{sw} (with 50% of switching probability). Depending on the magnitude of switching current, the dynamic behavior of MTJ can be divided into two regimes [25]: Sun model (I > I_{c0}) and Neel-brown model (I < $0.8I_{c0}$). The former is also called precessional switching which addresses fast switching (until sub 3ns) but consumes more energy with high current density. Reversely, the latter consumes less energy with low current density but leads to a slower switching which is called thermally-assisted switching. The two regimes are derived from the Landau-Lifshitz-Gilbert equation. τ_{sw} can be calculated as follows:

$$\tau_{sw} = \tau_0 \cdot exp\left[\frac{\Phi_b}{k_B T}\left(1 - \frac{I}{I_{c0}}\right)\right], \quad when\ I < 0.8I_{c0} \quad (4)$$

$$\frac{1}{\tau_{sw}} = \left[\frac{2}{C + ln(\frac{\pi^2\zeta}{4})}\right]\frac{\mu_B P_{ref}(I - I_{c0})}{em_m(1 + P_{ref}P_{free})}, when\ I > I_{c0} \quad (5)$$

where τ_0 is the attempt period, T is the temperature, k_B is the Boltzmann constant, C is the Euler's constant, ζ is the thermal stability factor, m_m is the magnetization moment, P is the tunneling spin polarizations. Usually a high current ($I > I_{c0}$) is applied to guarantee fast writing in memory. Meanwhile, MTJ can also be switched erroneously by relatively low current ($I < 0.8I_{c0}$) during a long period of reading operation, which determines the data retention time.

The thermal fluctuation of environment introduces the randomness in the switching process [19]. For $I > I_{c0}$, the switching probability can be described as follows [26]:

$$P_{sw} = exp\left\{-4 \cdot f \cdot \zeta \cdot exp\left[-\frac{2 \cdot (t_{pulse} - delay)}{\tau_{sw}}\right]\right\} \quad (6)$$

$$f = \left(\frac{2}{1 - \frac{I_{c0}}{I}}\right)^{\left(\frac{-2}{1+\frac{I}{I_{c0}}}\right)} \quad (7)$$

where t_{pulse} is the voltage pulse width, *delay* is a fitting parameter. The stochastic switching and process variation are integrated into the model by using the random functions in Verilog-A language [23]. The users are free to reconfigure the simulation conditions by choosing different types of statistical distributions for device parameters (t_{sl}, t_{ox}, TMR and average switching delay τ_{sw}). The variables used in the model are adjusted to achieve good agreement with the equation (6). Figure 4 demonstrates the switching probability as a function of pulse width.

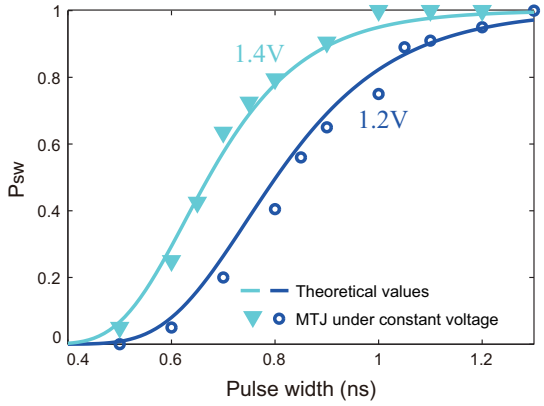

Figure 4: Switching probability P_{sw} as a function of pulse width: the lines are theoretical values plotted from (6) and the markers are statistical results from 1000 times of Monte Carlo simulation.

In order to get a configuration corresponding to experimental data, the users can set the MTJ physical parameters using the default values in Table 1. The bias conditions and circuit parameters are also listed in Table 1.

Table 1: Parameters and variables

Parameter	Description	Default Value
ΔH_k	Anisotropy filed	$113.0 \cdot 10^3 A/m$
M_s	Saturation magnetization	$1257.0 \cdot 10^3 A/m$
α	Magnetic damping constant	0.027
γ	gyromagnetic ratio	$1.76 \cdot 10^{11} rad/(s \cdot T)$
μ_0	permeability in free space	$1.257 \cdot 10^{-6} T/(m \cdot A)$
k_B	Boltzmann constant	$8.625 \cdot 10^{-5} eV/K$
T_0	Ambient temperature	300 K
Variable	Description	Default Value
t_{ox}	Thickness of oxide barrier	0.85nm
TMR(0)	TMR ratio with 0 stress voltage	150%
Area	MTJ surface	$40nm \cdot 40nm \cdot \pi/4$
t_{sl}	Thickness of free layer	1.3nm
V_{sl}	Volume of free barrier	Area $\cdot$ t_{sl}
RA	Resistance-area product	$5\ \Omega \cdot \mu m^2$
Circuit	Description	Default Value
V_{dd}	Supply voltage of PCSA	1V
V_{ddh}	Supply voltage of writing circuit	1V
$\frac{W_{min}}{L_{min}}$	Minimum transistor dimension	80nm/30nm

4. CIRCUIT DESIGN OF TRUE RANDOM NUMBER GENERATOR

The MTJ stochastic switching provides a new randomness source for TRNG. Based on unpredictable physical phenomenon, it can supply real random bitstreams by special circuit design. As shown in Figure 4, continuous switching probability can be obtained by tuning either the applied current or the stress time. A tunable switching current I_{sw} with 5ns pulse is applied in this work to investigate the switching probability. The simulation result presented in Figure 5 indicates that $I_{sw} = 84.5\mu A$ is required for a switching probability of 50%. Our compact model is based on a symmetrical MTJ (the critical current for P to AP is the same with that of AP to P).

With continuous scaling down of semiconductor devices, performance degradation induced by process variation becomes a critical issue in CMOS circuits and systems design [27]. Meanwhile, the limited fabrication precision of MTJ induces variable device parameters like the oxide barrier thickness t_{ox}, free layer thickness t_{sl} and TMR ratio [21]. In order to guarantee an accurate probability and high level of randomness, it is necessary to take into consideration the process variations.

In the considered 28nm FDSOI design kit, process variability is modeled by four worst-case corners [28]. TT is the typical compact model extracted from the "golden die" of the "golden wafer" representing the center-line process technology. On the one hand, the corner models are generated from slow nMOS and slow pMOS (SS) to model the worst-case speed, and from fast nMOS and fast pMOS (FF) to model the worst-case power. On the other hand, the corner models are generated from fast nMOS and slow pMOS (FS) to model the worst-case '1', and from slow nMOS and fast pMOS (SF) to model the worst-case '0' [29]. The worst-case corner models offer for designers capability to simulate the pass/fail results of a typical design and are usually pessimistic. The process variations of MTJ are also integrated in the compact model [23]. Using these models, two current values of worst cases (maximum(FF) and minimum (SS)) are obtained for the switching probability of 50% (shown in Figure 4).

With the obtained switching current, we propose a novel design of TRNG circuit. The general architecture is illustrated in Figure 6. It is composed of MTJ random writing part, pre-charge sense amplifier (PCSA) and correction block. By an appropriate choice of transistors dimensions, a particular switching probability can be obtained to get a

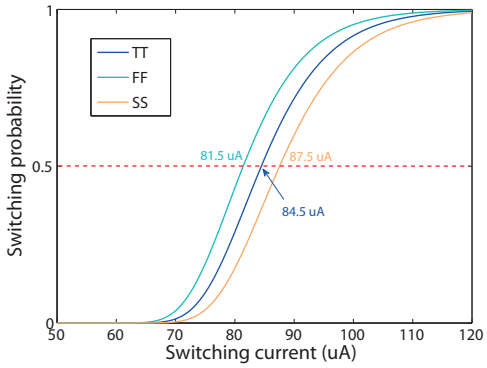

Figure 5: Switching probability of MTJs on function of switching current with 10ns pulse. The current with 50% switching success is indicated above. This figure is obtained by 1000 runs of Monte-Carlo simulation with the same MTJ under voltage pulses.

real random bitstream. In order to improve the reliability, a correction logic block composed of counters and comparator is implemented. This block generates a control signal to modulate the switching current, which guarantees the exact given probability of obtained random number bitstream (ideally with 50% of '1' and 50% of '0').

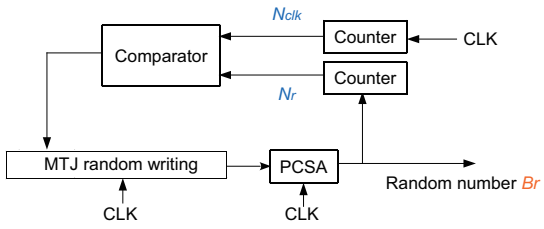

Figure 6: Architecture of proposed MTJ-based true random number generator: The random writing circuit generates a switching current to write the MTJs with 50% success and it is controlled by the correction block; The MTJ writing part enables MTJ switching (generating random number or resetting to initial state); The correction block composed of counter and comparator is used to execute real-time output probability tracking and send feedback to writing block.

The Analog part of writing and sensing blocks are displayed in Figure 7. The voltage-current converter (in the blue frame) generates a writing current for MTJ according to the random number probability obtained in the previous clock cycle. The transistors are configured to guarantee a switching probability of P_{sw}=50%. This circuit operates in three phases:

1) *Reset phase*: CLK='0', P_6 and N_6 are open while all of other transistors are closed. The two MTJs are switched to the initial state (MTJ is with low resistance) with a relatively high current (usually $>3I_{c0}$ which guarantees 100% switching probability).

2) *Random writing phase*: CLK='0', P_5 and N_5 are open to enable the MTJ switching with a certain current according to the required probability. When N_{c1} is open and N_{c0}, N_{c2} are closed, the switching probability of MTJ in the next step will keep 50%. If $P_{sw} > 50\%$, N_{c0} is open while the two others are closed to reduce writing success (with I_{sw}=81.5μA), resulting in decreased random probability. If $P_{sw} < 50\%$, N_{c2} is open and N_{c0}, N_{c1} are closed, thus the MTJ is more easily switched with a higher current flow (with I_{sw}=87.5μA). Consequently, the random probability will increase until 50%. During the first two phases, the sensing circuit is always at pre-charge phase and both outputs of PCSA (Q_m and $\bar{Q_m}$) are charged to V_{dd}.

3) *Sensing phase*: CLK='1', N_0, N_1, N_2, N_3, N_4 are open to drive sensing current flowing to the ground through MTJ0 or MTJ1. With resistance difference between the MTJ and the reference resistor (R_{ref}=(R_p+R_{ap})/2), the unbalanced current generates different discharge speeds. The lower resistance side discharges more quickly, and its output (Q_m or $\bar{Q_m}$) voltage will be pulled down to the ground, whereas that of the other branch will be pulled up to V_{dd}. Thus, the random number is obtained at the output. In order to guarantee the right probability, the random number bitstream is evaluated using counters and comparator. The evaluation result will generate a control signal which tunes the writing current in the next switching phase. The detailed phase transition diagram is illustrated in Figure 8.

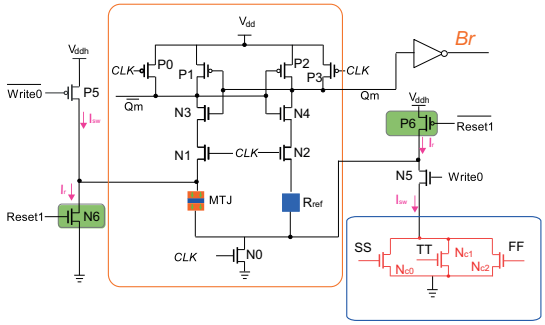

Figure 7: MTJ writing circuit and PCSA: I_{sw} is the switching current flowing through MTJ during random writing phase and I_r is the switching current during reset phase. N_{c0}, N_{c1} and N_{c2} modulate the switching current according to the random number probability obtained in the precedent cycle.

As a reliable sensing circuit is required, PCSA is utilized in this work because of its perfect performance in sensing latency and reliability [30,31]. Normally, sensing errors may be induced by the process variation of FDSOI CMOS and MTJ. In order to get an error-free PCSA, the dimension of all the transistors in PCSA is validated by 1000 runs of Monte Carlo simulations. Transistors N_1 and N_2 are implemented to avoid the crosstalk between writing and sensing circuit.

5. SIMULATION RESULTS

By using the FDSOI 28nm design kit and MTJ compact model, we carried out transient simulation of the proposed TRNG circuit. The corresponding time-domain diagram is presented in Figure 9. Firstly, the switching circuit starts to write with a relatively low current (84.5μA) with the condition of N_r=N_{clk}/2 (switching probability P_{sw}=50%). With $N_r > N_{clk}/2$, the switching probability is decreased while the control transistor N_{c0} is opened by the correction block. When N_r is smaller than $N_{clk}/2$, the switching current is increased with the control transistor N_{c2} activated by the

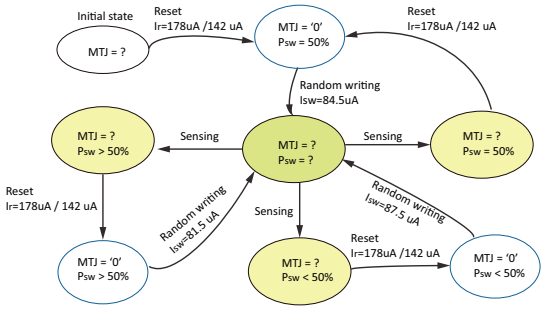

Figure 8: The phase transition diagram of proposed circuit design: The three states in blue frame are with different output random number probability after reset phase; The state in green signifies the unknown switching probability after random writing phase; The three states in yellow are with different known random number probability after sensing phase. For MTJs, '0' represents P state and the resistance is relatively low. '?' represents unknown information.

correction block. This simulation result matches well the aforementioned design goal and the functionality is well confirmed.

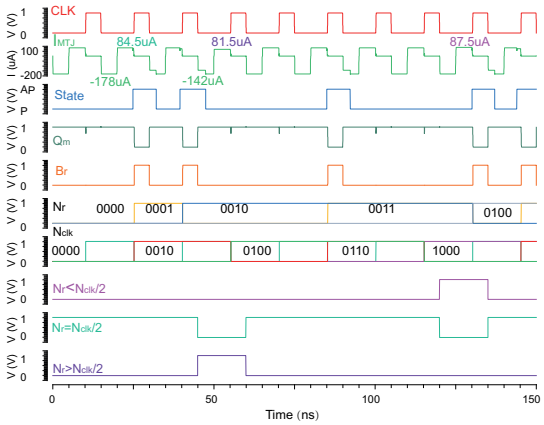

Figure 9: Time-domain diagram of proposed true random number generator. During each cycle, the MTJs are firstly reset to the initial state (with I_r=178μA for P state and I_r=142μA for AP state), then randomly switched, and finally sensed at the output. The initial current is set for 50% of switching success.

Based on the validated functionality, the circuit stability has also been estimated. The process variation of MTJs and transistors is taken into account by simulations with different cases of process variation. Figure 10 displays the probability of '1' in the obtained random bitstream during 100 cycles under different conditions. It is observed that the random number probability with different fixed-corner models becomes stable around 50% after 30 cycles. It is neccessary that the output bitstream probability needs to keep stable around 50%, which should pass the NIST test [32]. Our design has been proven to pass at least 12 tests among 15 using a 100 kbits sequence with different conditions of process variability.

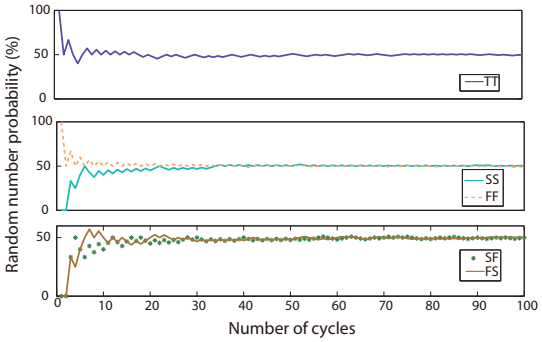

Figure 10: Output '1' probability versus number of clock cycles: The output random number probability becomes stable after 30 cycles (The probability of '1' occurrence stays around 50%) for all the five corner models.

Table 2: Comparison of performance in TRNG

	[10]	This work
Technology node	CMOS 90nm	FDSOI 28nm
Probability control	Digital	Analog
Estimated area	N/A	5.88 μm^2
Tuning steps	300	~30
Energy Efficiency	Not reported	1.25pJ/bit
Operation Frequency	66.6MHz	66.6MHz
Variability tolerance	N/A	high
NIST	N/A	pass

The detailed comparison of performance with the works in [10] is shown in table 2. It demonstrates the proposed design has smaller area (DAC is not used), shorter tuning steps (with short delay before generating stable random bitstreams). Moreover, the switching current of the MTJ in [10] is much higher than that of the MTJ in this paper, our PCSA is ultra low power, and the block DAC consumes much energy, our design can be estimated to have more power efficiency.

6. CONCLUSION

This work addressed circuit design for TRNG based on STT-MTJ, which has intrinsic stochastic effect. The proposed solution has been implemented with FDSOI CMOS circuits. Monte-Carlo simulations were performed to prove its feasibility and transient simulation has validated its functionality. Furthermore, the simulation with process variation of MTJs and transistors has proved the variability awareness of this design. The comparison with another similar work shows that the proposed design has better performance in terms of area, power efficiency, operation speed and variability tolerance. As an extension of this work, we will use this circuit to explore a new methodology for stochastic computing [33].

Acknowledgment

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