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Skyrmion-Induced Memristive Magnetic Tunnel Junction for Ternary Neural Network

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ABSTRACT Novel skyrmion-magnetic tunnel junction (SK-MTJ) devices were investigated for the first time to implement the ternary neural networks (TNN). In the SK-MTJ, an extra magnetoresistance state beyond binary parallel and anti-parallel MTJ states was achieved by forming a skyrmion vortex structure in the free layer. Based on the SK-MTJ, we propose a synaptic architecture with bit-cell design of $+1$, 0, and -1 to replace the full precision floating point arithmetic with equivalent bit-wise multiplication operation. To explore the feasibility of the SK-MTJ-based synaptic devices for TNN application, circuit-level simulations for image recognition task were conducted. The recognition rate can reach up to 99% with 5% device variation and an average power consumption of 29.23 μW.

INDEX TERMS Skyrmion, synapse, magnetic tunnel junction, ternary neural network.

I. INTRODUCTION

Ternary neural network (TNN) is a novel quantization scheme for addressing the storage and computational issues as inspired by the network pruning and parameter compression in the deep learning community [1]–[3]. With both synaptic weights and neuron activations quantized to -1, 0 and $+1$, TNN is capable of reducing the data volume with very little prediction accuracy degradation [4]. Benchmarks on different datasets show that the performance of TNN is only slightly worse than the full precision counterparts but significantly outperforms the analogous binary neural network (BNN) [5], [6]. Table 1 listed all the validation accuracies of networks with different precisions on different datasets. From Table 1, TNNs achieve state-of-the-art performance as FWN on the small scale datasets (MNIST and CIFAR-10) while beat BNN a lot.

TABLE 1. Validation accuracies of network with different precision*.

Symbol	MNIST	CIFAR-10	ImageNet (top-1)	ImageNet (top-5)
TNN	**99.35**	**92.56**	**61.8/65.3**	**84.2/86.2**
BNN	99.05	90.18	57.5/61.6	81.2/83.9
FWN**	99.41	92.88	65.4/67.6	86.76/88.0

* *Data is from Reference [5]*
** *FWN = full precision weights neural network*

On the large scale datasets (ImageNet), BNN and TNN both get poorer performance than FWN, while the accuracy gap between TNN and FWN is smaller. Besides, TNN is also hardware-friendly for the implementation of large-scale networks on specialized non-volatile devices as well as custom circuits [7]–[9].

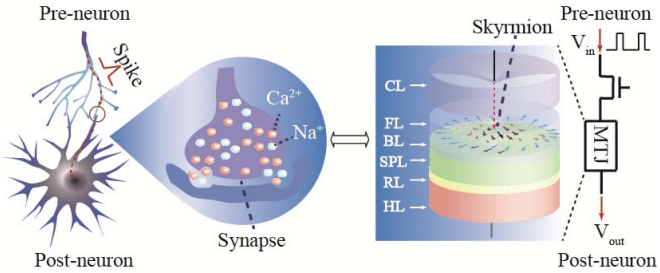


FIGURE 1. Analogy between the biological synapse and the electronic ternary synapse based on the SK-MTJ.

Among emerging non-volatile memory devices, magnetic random access memory (MRAM) has attracted world-wide attention due to desirable attributes like zero standby leakage, compatibility with CMOS and high integration density [10]–[12]. However, the binary switching property of MTJ between parallel (P) and anti-parallel (AP) states hinders the direct mapping of ternary synaptic weights to the bit cell under the TNN framework [13]. Although leveraging stacked MTJs [14] or using multi-level bit cells [15] might be alternatives, both of methods suffer from a challenge of a relative low tunnel magnetoresistance (TMR) ratio, which is a key limitation for high density and high reliability applications. To solve this dilemma, developing a novel MTJ with stable ternary states and high TMR is much preferable for the TNN framework.

In this paper, we propose a magnetic skyrmion-induced memristive MTJ (SK-MTJ) device with three-level states for ternary neural network. In this device, an intermediate skyrmion (SK) state was achieved and ternary weights could be represented in a bit cell synchronously. Similar to the biological synapse, the SK-MTJ could tune and keep its conductance due to the skyrmion generation and migration process [16], [17] when the input stimulus signal was received (Fig. 1). The SK-MTJ device is very suitable for designing artificial synapse in TNN due to the following features: the tunable resistance of intermediate state, low read/write current and high stability with double-protected skyrmion. In the rest of this paper, a detailed description of the SK-MTJ device design, the SK-MTJ based synapse cell design and the mapping of TNN into the SK-MTJ based synapse array will be presented.

II. DESIGN OF SK-MTJ DEVICE

A. SK-MTJ DEVICE DESIGN

The SK-MTJ device in this paper is comprised of Hard Layer (HL)/ Spacer/ Reference Layer (RL)/ Spacer/ Spin-Polarizing Layer (SPL)/ MgO/ Free Layer (FL)/ Capping Layer. Such a SK-MTJ device design is for the easy generation and stabilization of a skyrmion transformed from the domain wall (DW) in the FL. The split pinned layer (PL) that consists of SPL, RL and HL will exert inhomogeneous a stray fields B_s which could be divided into two components: the out-of-plane component $B_{S\perp}$ close to the edge of the FL and the in-plane component $B_{S/\!/}$ stray field at the

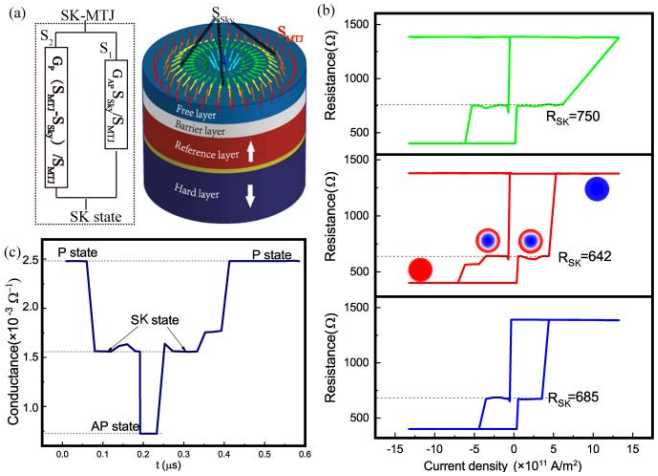


FIGURE 2. (a) Equivalent model of SK-MTJ device under the SK state; (b) time-resolved change of the conductance in the SK-MTJ device; (c) resistance variation of SK-MTJ under different DMI and B_s. Green line for strong B_s and $D = 1.25\text{mJ/m}^2$, Red line for moderate B_s and $D = 1.75\text{mJ/m}^2$, Blue line for moderate B_s and $D = 1.25\text{mJ/m}^2$.

center of the FL. Because of the presence of the inhomogeneous distribution of the B_s, the magnetic reversals of the FL in the two opposite directions show different processes [18]. The P-to-AP reversal starts with a domain wall (DW) nucleation from the center, and then expands to the whole FL processes. For the P to AP reversal, the edge was fixed by the $B_{S\perp}$. If a small nucleation occurs in the center, the orientation of the magnetization of the DW around the nucleation point is determined by the sign of D. If the D is negative, the nucleation in the center is favored by $B_{S\perp}$ and $B_{S/\!/}$ [19].

In this asymmetric reversal cycle, the generated domain bubble is unstable and will spontaneously collapse under the Laplace pressure P induced by DW surface energy [20], as shown by Eq. (1):

$$P = \sigma_{DW}/R \tag{1}$$

where σ_{DW} is the DW surface energy and R is the radius of the domain bubble area. With the aid of Dzyaloshinskii-Moriya interactions (DMI), the σ_{DW} will be reduced to a very low level and the skyrmion is more likely to be formed and detected [21], as described by Eq. (2):

$$\sigma_{DW} = 4\sqrt{AK_{eff}} - \pi D \tag{2}$$

where A is the exchange stiffness, K_{eff} is the effective anisotropy energy, and D is the DMI constant. Meanwhile, the distributed B_s will exert a pressure to balance the decreased P. Obviously, the formed skyrmion was double-protected by both the DMI and B_s, which is the main reason for its superior stability than skyrmion nucleated in multi-layer thin film with topological protection [22]. Such stability is advantageous for MTJ based artificial synapse design to increase nonvolatility and endurance. In addition, the critical current to generate the skyrmion state in the FL is quite low, which is favorable for low-power operation.

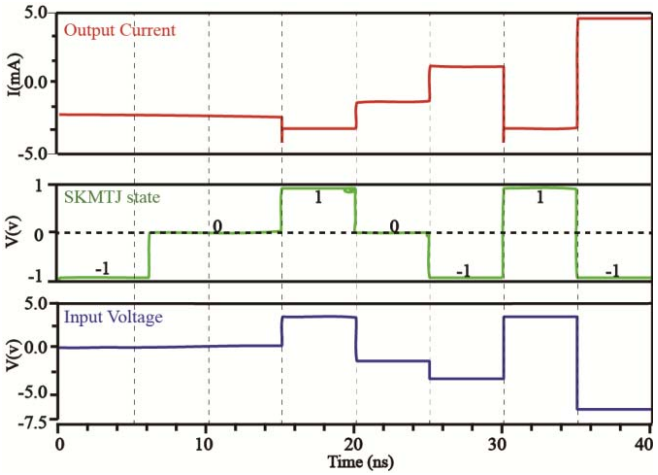


FIGURE 3. Transient waveforms of the SK-MTJ circuit model under different input voltages.

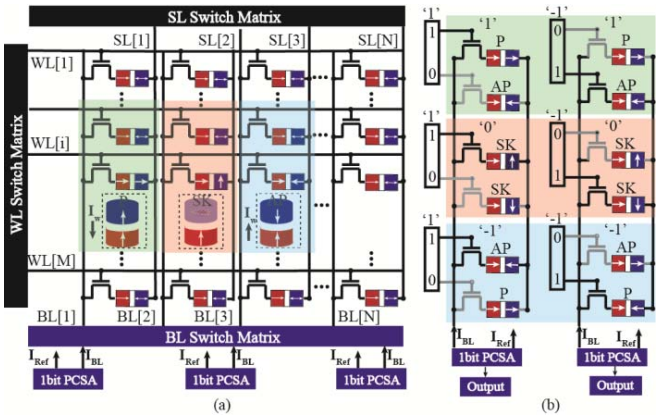


FIGURE 4. (a) Proposed SK-MTJ based pseudo crossbar array architecture; (b) The customized bit-cell design for SK-MTJ. The direction of the write current I_w flowing from PL to the FL is defined as positive.

B. MEMRISTIVE BEHAVIOR OF SK-MTJ

To verify the ternary states and memristive behavior of SK-MTJ, micromagnetic study of the reversal processes in the FL was performed by considering the DMI and the damping-like spin-transfer torque (STT) on the platform of Mumax3. The simulation results are shown in Fig. 2. When a skyrmion is formed in the region of the FL, the SK-MTJ can be regarded as two conductance S_1 and S_2 in parallel, as shown in Fig. 2(a). The conductance of the SK state G_{sk} was calculated by Eq. (3):

$$G_{SK} = (G_{AP} - G_P)S_{Sky}/S_{MTJ} + G_P \tag{3}$$

where G_{AP} and G_P are the conductance of the AP and P states without a skyrmion, S_{Sky} was the area of the skyrmion and S_{MTJ} was the area of the SK-MTJ. In this case, S_{MTJ} could be regarded as a constant while S_{Sky} was decided by the DMI and B_s as depicted in Eq. (1) and Eq. (2).

In Fig. 2(b), a stable SK state was found and the impact of the input current on the resistance of the SK state with respect to different D and B_s values was depicted. With different external parameters, the resistances of different SK states were calculated to be 750Ω, 642Ω and 685Ω under a uniform TMR of 245%, respectively. This could be explained by the fact that the size of a skyrmion was influenced by the synergistic effect of DMI and vertical component of B_s as indicated in Eq. (1) and Eq. (2). As DMI and B_s could be tuned by the thickness of MgO and the PL constitution, the design of the SK-MTJ device is highly flexible to meet different application requirements. Specially, the SK-MTJ with moderate B_s and $D = 1.75mJ/m^2$ was selected to study the conductance variation and transformation method between the three states. As shown in Fig. 2(c), the conductance of the two SK states in an asymmetric cycle were the same, which was attributed to the same S_{Sky} of skyrmion. SK-MTJ demonstrated a current-induced memristive behavior with three-level states, which make it possible to support the neural signal transmission via the write and read operation in the synapse array.

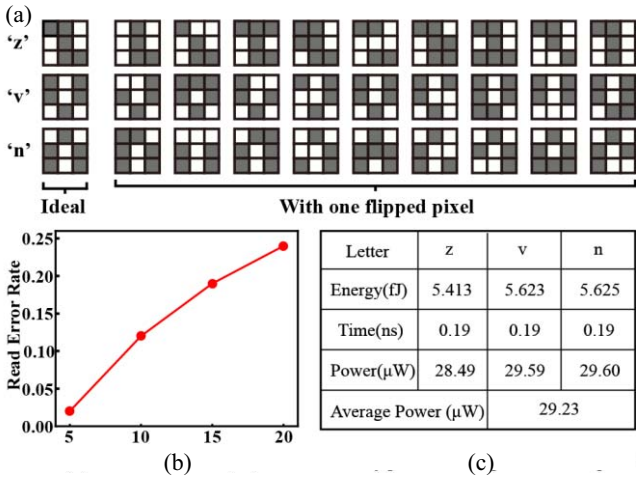
Then, a compact circuit model was developed in Verilog-A language and utilized to illustrate the memristive behavior of SK-MTJ for circuit simulations. The developed SK-MTJ model was tested in a test circuit based on a 40 nm technology. As shown in Fig. 3, with different input voltages, the conductance of SK-MTJ will change between three states and will keep unchanged until the next valid signal arrival. All the six interconversions between the three states could be completed when the input signal is beyond a certain threshold. Such memristive behavior will make the write and read operation possible to support the weight update in the synapse array.

III. SK-MTJ BASED TNN

A. SK-MTJ BASED SYNAPSE CELL

Based on the circuit model, we monolithically integrated a SK-MTJ and an access transistor (refer to 1T-1MTJ design) in a $M \times N$ pseudo crossbar array as shown in Fig. 4(a). Before the encoded pattern fed into the array, there will be one-time programming operation to initialize all the cells. For example, if P state was to be written to cell [i][1], the WL (word line) [i] was first activated so that a positive current I_w (FL to PL) can pass from the SL (source line) [1] to the BL (bit line) [1] through the transistor. The same situation was suitable for writing weight AP state but with a negative I_w.

Fig. 4(b) presents the principle of the proposed bit-cell design for SK-MTJ. For each synaptic weight, +1 is represented by two cells where the top one is in P and the bottom one is in AP. The reversed pattern is used for −1, while 0 is represented by two cells both in SK. The input pattern was fed into the bit-cell with two adjacent WLs in complimentary state where (1, 0) denotes '1' and (0, 1) denotes '−1'. Then, the output of one bit-cell could be represented by the value of the flowing current which depends on the bit-wise multiplication operation of the input pattern and bit-cell pattern. For example, when input vector is −1, for the cell of weight



Letter	z	v	n
Energy(fJ)	5.413	5.623	5.625
Time(ns)	0.19	0.19	0.19
Power(μW)	28.49	29.59	29.60
Average Power (μW)	29.23		

FIGURE 5. (a) Image patterns of letter 'z', 'v' and 'n' for training and testing; (b) Recognition error rate vs and device variation; (c) Key parameters for calculating energy consumption.

−1, the cell in the activated row is in P, leading to a large cell current, which can be regarded as a bit-wise output of '+1'. For the cell of weight 0, the cell in the activated row is in SK state, leading to an intermediate cell current, which can be regarded as a bit-wise output of '0'. The weighted sum can be counted as the accumulated current on the BL (I_{BL}) in each column while the I_{Ref} is used as the reference current. By comparing the I_{BL} and I_{Ref}, its output can be directly regarded as the binary neuron output. For example, when a weighted sum is negative, i.e., the number of the I_{BL} is smaller than I_{Ref}, generating an output "−1", which represents that there are more "−1" than "+1" along the column, and vice versa.

B. SK-MTJ BASED TNN ARRAY

With the proposed SK-MTJ synapse and the pre-charge sense amplifier (PCSA) neuron [23], TNN array was employed for circuit simulations on 30 image patterns [24] consisting of three stylized letters ('z', 'v', 'n') as shown in Fig. 5(a). For implementation of the proposed SK-MTJ in large scale TNN, the impact of device variation on the recognition error rate was investigated. As shown in Fig. 5(b), the read error rate was less than 1% with 5% device variation and will increase linearly. This degradation will be mitigated with MTJ device fabricated with large TMR [25]. For energy-efficiency, the SK-MTJ based TNN achieves a low power consumption of 29.23μW during the whole simulation process. As for different letters, the corresponding input voltage vectors are different. Thus, we have to calculate the recognition energy for different letters solely and then add them up. All of the key parameters such as energy for each letter and simulation time constant are summarized in Fig. 5(c).

IV. CONCLUSION

In this letter, we propose for the first time a ternary SK-MTJ device to emulate the core synaptic functionality for TNN. The SK-MTJ overcomes the inherent binary constraint of typical MTJ and can be directly mapped into the TNN framework. Moreover, current-induced resistance adjustability of the SK state endows great flexibility when designing synapse. Our evaluations prove the feasibility of the proposed SK-MTJ based TNN for image recognition. This work suggests new possibilities for exploiting skyrmionic devices in DNN beyond typical racetrack memory.

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