Demonstration of Multi-State Memory Device Combining Resistive and Magnetic Switching Behaviors

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***Abstract*— Resistively enhanced magnetic tunnel junction (Re-MTJ) nonvolatile memory devices with a heterogeneous structure of an MTJ surrounded by resistive filaments were investigated for the first time for multi-level cell memory applications. By independent control of the MTJ and the conductive filaments, multi-state resistances can be obtained since both resistive and magnetic switching can be accomplished in a single element. Compared with the conventional MTJs, the Re-MTJ devices have more resistance states without increasing the dimension. The advanced logic-in-memory applications can also be enabled by using conductive filaments and MTJs for logic and storage, respectively. A direct proof of concept was demonstrated by the experimental realization of memory encryption function using Re-MTJ devices with transparent feature.**

***Index Terms*— Magnetic tunnel junction (MTJ), multi-level cell, logic-in-memory, nonvolatile memory, spintronics.**

I. Introduction

THE Moore's law is approaching the physical limit due to the increasing leakage current for the past decades. The emerging nonvolatile memories (NVMs) have the prospective for the extension of Moore's law with low power consumption, excellent scalability, fast access speed and high endurance. In particular, the NVMs with multi-state resistance behavior have attracted extensive attention for its potential in brain-inspired computing and advanced logic-in-memories. For example, multi-state NVMs have been used to construct the memristive logic computation [1], [2] and neuromorphic networks [3]–[5], which offer an opportunity to circumvent the "von Neumann bottleneck" in modern computer architecture.

Researchers have proposed some prospective ideas, such as spintronics memristor [6] and domain wall based MRAM devices [7], [8], which can be used to obtain multi-state resistances. In addition, several emerging NVM technologies, including resistive random access memory (RRAM) [3], magnetic random access memory (MRAM) [9], phase change memory (PCM) [2] and ferroelectric memory (FeRAM) [5], have attracted much attention from both industry and academia. Among those NVMs, RRAM and MRAM are two promising candidates with excellent endurance and scalability characteristics for realizing the multi-level cell [10]–[12]. For RRAM device with a metal-insulator-metal (MIM) structure, the resistance can be switched between low-resistance state (LRS) and high-resistance state (HRS) by configuring the conductive filaments with different bias voltages [13]. The stochastic nature related to the filament configuration leads to multi-state resistances; however, it suffers from relatively low access speed [2], [9]. Regarding an MRAM device, e.g., magnetic tunnel junction (MTJ), it consists of an oxide tunneling barrier between two ferromagnetic layers and the device resistance can be switched by changing the relative magnetizations (either parallel, P, or antiparallel, AP) of the ferromagnetic layers via a magnetic field or a current [14]–[16]. The multi-state resistance behavior can be also achieved by either using the intrinsic stochastics of magnetic switching or using vertical stacked MTJs. However, both methods are challenged by a relative low tunnel magnetoresistance (TMR) ratio.

In this letter, we have investigated a resistively enhanced magnetic tunnel junction (Re-MTJ) device that can be used to construct the multi-level cell. The independently-controlled resistive switching and magnetic switching as well as the multi-state resistance behavior were presented in the transport measurements. The state transition diagrams of Re-MTJ device under a combination of a voltage and in-plane magnetic fields were discussed. A proof-of-concept demonstration of NVM encryption was experimentally realized using the fabricated Re-MTJ devices with transparent feature.

II. Experiments

The magnetic films consisting of substrate/Ta(5nm)/Ru(15nm)/Ta(5nm)/Ru(15nm)/Ta(5nm)/Ru(5nm)/PtMn(20nm)/CoFeB(1.5nm)/CoFe(2nm)/Ru(0.85nm)/CoFeB(1.5nm)/CoFe

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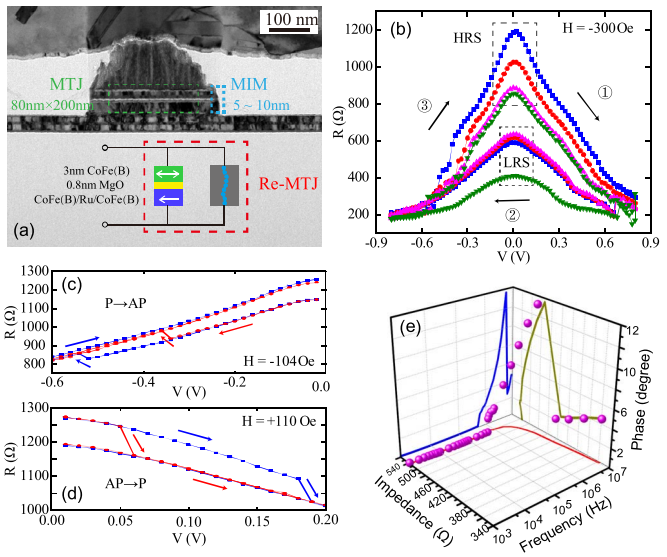


Fig. 1. (a) Cross-sectional HRTEM image and the corresponding device model of Re-MTJ. The Re-MTJ has a device structure of an MTJ in parallel connection with an MIM. The blue balls represent the conductive filaments; (b)-(d) Transport measurements show both the resistive switching as (b) and magnetic switching as (c) and (d); (e) AC-impedance spectroscopy of the device at 20 mV.

(1.5nm)/MgO(0.8nm)/CoFe(1.5nm)/CoFeB(1.5nm)/Ru(2nm)/Ta(5nm)/Ru(10nm) were sputtered onto SiO_2-coated Si wafers and annealed under an in-plane magnetic field. The MTJ multilayers were patterned into ellipse-shaped nanopillars with a dimension of 80×200 nm^2. The nanopillars were then encapsulated by a SiO_x-based polymer in a low temperature curing process below 300 °C. More details for the device fabrication can be found in our earlier work [17].

The electrical measurements were performed using a Keithley-4200 CVU semiconductor analyzer, which is capable of carrying out both direct current (DC) transport and alternating current (AC) impedance measurements in a frequency range of 10^3 Hz to 10^7 Hz. Here, a two-probe geometry is utilized for all the measurements at room temperature. The bias voltages with the duration of 200 ms were applied to the top electrode of the device, while the bottom electrode was grounded. An in-plane magnetic field with a precision below 1×10^{-3} Oe was utilized during the measurements.

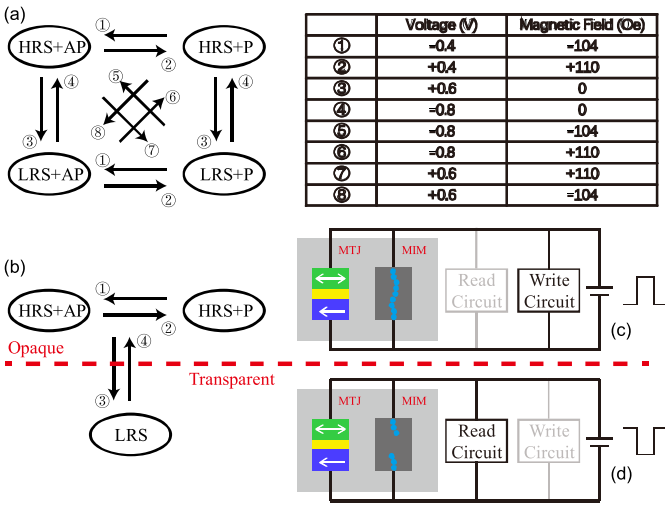
III. Results and Discussion

The proposed Re-MTJ device has a heterogeneous structure with a parallel connection of an MIM (conductive filaments) and an MTJ, as shown in the Fig. 1(a). The electrons can either pass the MgO barrier of MTJ by tunneling, or go through the conductive filaments via hopping. The conductive filaments are located at the edge of MTJ nanopillar in SiO_x matrix and have been directly observed in previous studies [17]–[19]. Those conductive filaments favor either an electrochemical reduction process of $SiO_x \rightarrow$ Si (i.e., set process) under a positive voltage or an inverse Joule-heating assisted process of Si $\rightarrow$ SiO_x (i.e., reset process) under a negative voltage [20], [21].

Different types of multi-state resistance behavior in Re-MTJ can be observed from the switching process. The resistive and magnetic switching of Re-MTJ device are presented in transport measurements in Fig. 1(b), 1(c) and 1(d). In the resistive switching, a set (reset) voltage of about $+0.7$ V (-0.8 V) can switch the MIM into LRS (HRS). Meanwhile, a magnetic switching of the MTJ between AP and P state occurs under voltages lower than ± 0.5 V. By applying appropriate magnetic fields and voltages, two switching mechanisms can be independently controlled in Re-MTJ devices. Fig. 1(b) shows four resistive switching loops with different HRS and LRS resistances. Here, in order to eliminate the influence of magnetic effects, a large external magnetic field (much larger than the coercivity of the free layer of MTJ) was applied to pin the state of MTJ. Similar to filamentary-based oxide RRAM devices, the Re-MTJ can present one type of multi-state resistance behavior due to the different configuration of the filaments. The magnetic switching with spin transfer torque (STT) effect can occur randomly for both P to AP and AP to P process, as shown in Fig. 1(c) and 1(d), respectively. In order to avoid the influence of resistive behavior, the voltages were well controlled below the threshold of the resistive switching. The in-plane magnetic fields (lower than the coercivity of the free layer) are used to reduce the critical currents and are not indispensable for STT switching in practical [10]. A TMR ratio of $\sim$ 20% together with an ON/OFF ratio of bipolar resistive switching up to 100 can be obtained from the measurements and the compact model simulation of Re-MTJ [17].

Interestingly, by a combination of resistive and magnetic switching, another type of multi-state resistance behavior can be obtained beyond the stochastic feature of conductive filaments. In details, for MTJs in both AP and P states, more resistance states can be accomplished with different configurations of conductive filaments. Since the filaments are only existed in a region of 5-10 nm around MTJ nanopillar [17], the Re-MTJ devices can provide more resistance states and better stochastic behavior without extra expense on the area of device compared to conventional MTJs. In addition, regarding the capacitor-like structure of resistive component, Fig. 1(e) shows the AC-impedance spectroscopy of the Re-MTJ device. The phase degree as a function of frequency maintains a relative small range from 0° to 2.5° with the frequency up to 10^6 Hz, which indicates a good stability of Re-MTJ device for potential applications in logic/computation [22]. We note that the deterioration of stability in higher frequency may be explained by the parasitic capacitance; which is probably formed on the edges of nanopillar during the etching process. However, it barely shows the influence on a good nonvolatility of Re-MTJ device [17].

The independent control of resistive switching and magnetic switching enables the Re-MTJ as a logic-in-memory device. Fig. 2(a) and 2(b) present the state transition diagrams of Re-MTJ device under a combination of a voltage and in-plane magnetic fields. Here, the purpose of utilizing a magnetic field is to clearly differentiate between the resistive and magnetic switching process. Regardless of stochastic behaviors, four different resistance states can be achieved as outputs, while the voltage and magnetic field can be used as two corresponding inputs. The results of logic computing can be stored in a combination of MTJ states (e.g. P or AP) and filaments configuration (e.g. HRS or LRS).



	Voltage (V)	Magnetic Field (Oe)
①	-0.4	-104
②	+0.4	+110
③	+0.6	0
④	-0.8	0
⑤	-0.8	-104
⑥	-0.8	+110
⑦	+0.6	+110
⑧	+0.6	-104

Fig. 2. The state transition diagrams of Re-MTJ device under a combination of voltage and magnetic field. (a) Four resistance states with a combination of configuration of conductive filaments (HRS or LRS) and MTJ (AP or P); (b) Three resistance states for ignoring MTJ states when the conductive filaments are on (LRS). (c) Writing and (d) reading operation of Re-MTJ device for the application as encryption memory.

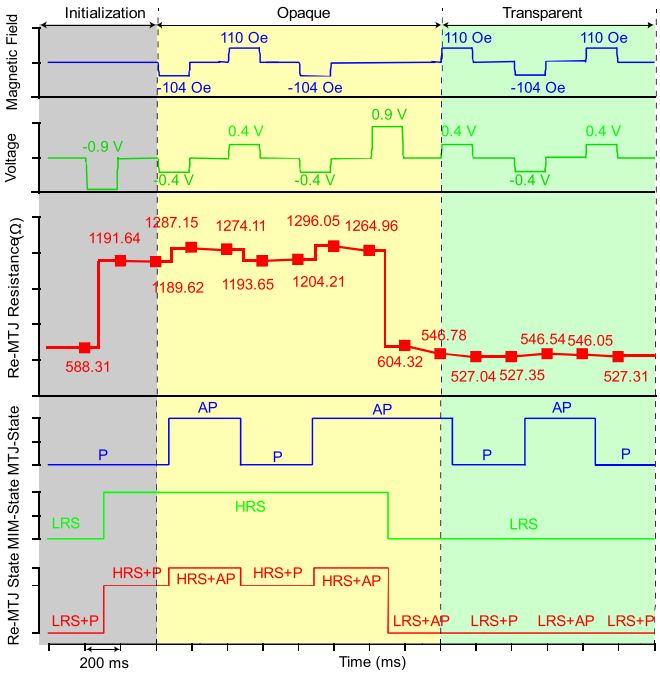


Fig. 3. Experimental demonstration of the functional behavior for memory encryption enabled by Re-MTJ device with transparent feature.

Furthermore, due to the parallel connection of MTJ and MIM, the difference of resistances between LRS+AP and LRS+P are lower than the counterpart between HRS+AP and HRS+P. By setting the appropriate judgments for peripheral sensing circuit, we can combine these two states (LRS+AP and LRS+P) together and treat Re-MTJ as a three-state device for simplicity. As shown in Fig. 2(b), when the MIM is in LRS, the conductive filaments are on and the small difference of resistances between AP and P states will be ignored by read circuit. Then the Re-MTJ is defined to be in the "transparent" mode, for the fact that the MTJ seems not existent. When the MIM is in HRS, the conductive filaments are off and the difference of resistances between AP and P states is large enough to be detected by read circuit. Then we can define that the Re-MTJ is in the "opaque" mode. In this context, the logic function, as a selector of whether the MTJ is readable or not, is accomplished by controlling the configuration of conductive filaments while the information is stored in MTJ.

This so-called transparent feature makes Re-MTJ an ideal device for realizing the function of NVM encryption. It's of great importance for NVM encryption since the information will be kept after powered off, which enables an attacker to extract the sensitive information from the memory with physical access to the system [23], [24]. The schematics of write and read circuits are presented in Fig. 2(c) and 2(d), respectively. As shown in Fig. 2(c), after storing the information into MTJ, a positive voltage pulse will be applied to Re-MTJ device and then, the MIM will be set as LRS. In this situation, the information is encrypted and cannot be read out. Therefore, a decryption process will be needed before the next reading operation. To retrieve the information, a negative pulse will be applied to Re-MTJ device and the MIM will be reset as HRS, as presented in Fig. 2(d). Then the MTJ will become readable and the information is decrypted. After the reading operation, the information will be encrypted again for data security.

A proof-of-concept of NVM encryption using Re-MTJ devices with transparent feature was experimentally demonstrated at room temperature. As shown in Fig. 3, the data is stored in MTJ by the magnetic field assisted STT effect, and the conductive filaments controlled by voltages provide a mechanism for data encryption. A -0.9 V voltage pulse resets the MIM to HRS and then the magnetic switching (AP/P) of the MTJ is readable with a resistance difference of $\sim 100\Omega$ between two states (i.e., HRS+AP and HRS+P). Otherwise, a $+0.9$ V voltage pulse sets the MIM to LRS and then the magnetic switching (AP/P) of the MTJ become transparent with the resistance difference of only $\sim 30\Omega$ between two states (i.e., LRS+AP and LRS+P). We note that the resistance difference between HRS+AP and HRS+P can be further improved by the optimization of the device structure and materials, e.g. utilizing a double MgO-based MTJ with tungsten (W) capping layers [25].

IV. Conclusion

In this work, we discussed a resistively enhanced MTJ (Re-MTJ) device which can be used for constructing the multi-level cell. The fabricated Re-MTJ devices displayed stable multi-states due to a combination of magnetic and resistive switching in a single element. Besides the storage function as NVM, those two independently-controlled switching mechanisms enable the Re-MTJs as logic-in-memory devices. A proof-of-concept of memory encryption was experimentally demonstrated using Re-MTJ device with transparent feature. Therefore, the Re-MTJ devices has promising applications in brain-inspired computing and advanced logic-in-memories.

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