Fast Vectorless Power Grid Verification using Maximum Voltage Drop Location Estimation*

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Abstract - Power grid integrity verification is critical for reliable chip design. Vectorless power grid verification provides a promising approach to evaluate the worst-case voltage fluctuations without the detailed information of circuit activities. Vectorless verification is usually required to solve numerous linear programming problems to obtain the worst-case voltage fluctuation throughout the grid, which is extremely time-consuming for large-scale verification. In this paper, a maximum voltage drop location estimation approach is proposed for efficient vectorless verification. The power grid nodes are grouped into disjoint subsets, and an estimation strategy is utilized to roughly locate the nodes which have the worst-case voltage drop in each group. Consequently, the verification problem size can be significantly reduced compared with accurate verification. Experimental results show that the proposed approach can achieve remarkable speedups with acceptable accuracy loss.

I INTRODUCTION

The design quality of the on-die power grid has a direct impact on chip performance and reliability. A well-designed power grid should provide sufficient power supply to all transistors on the chip and guarantee a certain noise margin during all possible circuit operations. As the supply and threshold voltages are decreased for lower power consumption and better performance in high performance circuits design, the functionality and performance of modern integrated circuits are becoming more and more vulnerable to power supply noises. Hence, power grid verification has become a crucial procedure to ensure a reliable chip design.

Traditional simulation-based power grid verification techniques suffer from the prohibitively high computation cost in enumerating an extremely large number of possible input current patterns. Another disadvantage of these methods is that early-stage verification cannot be performed since detailed information about the current waveforms is still unavailable. To overcome these issues and enable early stage power grid verification, a series of vectorless power grid verification techniques has been proposed in [1], and further studied in [2-10]. These approaches adopt the notion of current constraints to capture the circuit uncertainty at an early design stage, and evaluate the worst-case voltage fluctuations on each grid node by solving linear programming problems under the feasible space specified by these current constraints. In recent years, great efforts have been made to reduce the computation cost of vectorless power grid verification. Hierarchical matrix inversion algorithm [5] and $\mathcal{H}$-matrix-based approximate matrix inversion algorithm [7] is proposed to speed up the sub-problem of linear system solution. A convex dual algorithm [4] is proposed to speed up the sub-problem of linear programming solution. The sparse approximate inverse (SPAI) technique is proposed in [3] to accelerate the matrix inversion problem as well as reduce the number of variables in linear programming problems. However, the computation cost is still too high to be practical in the prototype vectorless power grid verification framework due to the extremely large number of linear programming problems that need to be solved. So there are also several research works to improve the verification efficiency. A geometric approach is introduced in [6], a selected inversion approach is proposed in [8], and a partial differential equation (PDE) constrained optimization based multilevel verification framework is proposed in [9].

In this paper, we propose a new efficient vectorless power grid verification framework. Major contributions of this paper are listed as follows:

1) We present a maximum voltage drop location estimation algorithm. For a group of power grid nodes which are properly selected, the proposed algorithm can find out the possible nodes which may have the maximum worst-case voltage drop without the accurate calculation of the exact worst-case voltage drops at each node in this group.
2) Based on the location estimation technique, we propose a modified framework for vectorless power grid verification. In this framework, power grid nodes are checked in a group-by-group manner. We first try to pick out the possible "worst" power grid nodes in a certain group, and then perform accurate verification on these nodes. By following this strategy, the number of power grid nodes which need accurate verification is effectively reduced, and thus the overall vectorless power grid verification becomes much more efficient.
3) Since the accuracy of the maximum voltage drop location estimation algorithm depends to some extent on the grouping method for selecting the nodes which will be analyzed in one group, we propose a modified algebraic circuit partitioning technique which has a better ability to deal with the impact of VDD pads than methods that simply adopt existing graph partitioning algorithms to decompose the power grid.

The rest of this paper is organized as follows. Power grid modeling and prior vectorless power grid verification

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methods are summarized in Section II. Details of the proposed approach are presented in Section III. Experimental results are provided and analyzed in Section IV. Concluding remarks are given in Section V.

II. BACKGROUND

A. Power Grid Model

The modeling methods have a strong influence on the power grid verification methodology. For RC model, since voltage levels can only be inferior to VDD, we just need to check that the voltage on every node of the power grid does not drop by more than some critical threshold. However, for RLC model, the presence of inductances can cause the voltage on a given node to fluctuate in both directions, either increasing or decreasing, which makes the power grid verification problem more complicated.

With RC model in [1], each branch of the power grid is represented as a resistor and there is a capacitor from every grid node to ground. Let $\mathrm{v}(t)$ be the vector of voltage drops, and $\mathrm{i}(t)$ be the vector of current excitations. Then according to [1], the following system equation which describe the functional relationship between voltage drops and current excitations must be satisfied,

$$G\mathbf{v}(t) + C\mathbf{v}'(t) = \mathbf{i}(t) \tag{1}$$

where G is an $n \times n$ conductance matrix and C is an $n \times n$ diagonal matrix of node capacitances.

An RLC model is introduced in [2]. In this model, each branch of the power grid is represented either by a resistor, referred to as an r-branch, or by a resistor in series with an inductor, referred to as an rl-branch. The system equations can be written as:

$$G\mathbf{v}(t) + C\mathbf{v}'(t) - M\mathbf{i}(t) = \mathbf{i_S}(t) \tag{2}$$

$$M^T\mathbf{v}(t) + L\mathbf{i}'(t) = 0 \tag{3}$$

where M is an $n \times m$ incidence matrix whose elements are either ±1 or 0, and L is an $m \times m$ diagonal matrix of inductance values.

B. Current Constraints

To address the requirement of early-stage power grid verification, the framework of current constraints which defines a feasible space of current excitations is adopted by vectorless power grid verification algorithms to capture the circuit uncertainty at the early design stage.

There are mainly two kinds of current constraints used in the existing vectorless power grid verification algorithms: local constraints and global constraints. Local constraints define upper bounds on individual current sources,

$$0 \le \mathbf{i}(t) \le \boldsymbol{I_L} \quad \forall t \ge 0 \tag{4}$$

where $\boldsymbol{I_L} \ge 0$ is an $n \times 1$ upper bound vector. Global constraints define upper bounds for certain groups of current sources,

$$U\mathbf{i}(t) \le \boldsymbol{I_G} \tag{5}$$

where U is an $m \times n$ matrix which contains only 0s and 1s and $\boldsymbol{I_G} \ge 0$ is an $m \times 1$ upper bound vector.

These current constraints give DC upper bounds on transient waveforms. If the upper bounds are also defined by a set of transient waveforms, the result of the vectorless power grid verification may be more realistic while the involved problems will be more difficult to solve. In [10], hierarchical current and power constraints are used to represent the transient constraints approximately.

C. Vectorless Power Grid Verification

Vectorless power grid verification aims to check the safety of the power grid by estimating the worst-case voltage fluctuations under given current constraints. By establishing a computable explicit expression for the vector of maximum node voltage fluctuations, vectorless power grid verification boils down to solving linear programs which depend on a certain matrix inverse. In [1], a DC model of the power grid is used to give an upper bound of the voltage drops in the corresponding RC model. So the upper bound of the worst-case voltage drop vector can be evaluated as follows:

$$\mathbf{v}_{max}(t) = emax_{\forall \mathbf{i} \in \mathcal{F}}(G^{-1}\mathbf{i}) \tag{6}$$

where the notation $\mathrm{emax}(\cdot)$ means an element-wise maximization. For the same RC model, a more careful analysis is given in [6], which results in a tighter upper bound:

$$\mathbf{v}_{max}(t) = (I + G^{-1}\frac{C}{\Delta t})emax_{\forall \mathbf{i} \in \mathcal{F}}(A^{-1}\mathbf{i}) \tag{7}$$

where $A = G + C/\Delta t$. Upper and lower bounds of the voltage fluctuations in the RLC model are analyzed in [2].

Most of the existing approaches aim to compute the worst-case voltage fluctuation for each node by solving linear programming problems which is time-consuming for large-scale power grids. A geometric approach is introduced in [6]. By exploiting particularities of the power grid at design time and the geometry of current feasibility space, the solution of the vectorless verification problem is reduced to a user-limited number of linear system solutions. In [9], a scalable multilevel vectorless power grid verification framework based on the key ideas of multilevel PDE-constrained optimization methods is proposed. By taking advantage of a series of coarsest to coarser grid verifications, the finest power grid verification can be accomplished in a more efficient way. The selected inversion in [8] selectively constructs the matrix inverse by exploiting the grid locality and constraint locality to improve the inversion efficiency and also speedup the linear programming which can provide a possible way for the large-scale power grid verification.

III. PROPOSED APPROACH

A. General Framework

In this paper, we mainly discuss the RC power grid model in which only the IR drops need to be considered. We will first use the upper bound defined by (6) to show how the proposed algorithm works since it is relatively simpler. And then we will also give some explanation about how to handle the more complicated upper bound defined by (7).

To guarantee the safety of the power grid, we should check that the worst-case voltage drop of every power grid node does not exceed some critical threshold. Since the up-

per bound of the worst-case voltage drop vector defined by (6) includes an element-wise maximization notation, most vectorless power grid verification algorithms also follow the element-wise checking strategy, i.e., these methods compute the worst-case voltage drops for every node on the grid. However, if we can filter out the nodes which have relatively smaller worst-case voltage drops in advance, the computation cost of the whole vectorless verification will be reduced. For example, it is easy to see that all the power grid nodes with no current source attached cannot have the maximum worst-case voltage drop in the DC model since given an arbitrary waveform combination, only the nodes that have current sources connected to ground can become the "worst" power grid node, i.e., the node which has the maximum voltage drop.

The main idea of this paper is to give a generalized method to pick out the power grid nodes which may have the maximum worst-case voltage drop. The vectorless power grid verification can be viewed as a maximization problem:

$$\textit{Maximize} \quad v_{max} = max\ \{v_{max_1}, v_{max_2}, \cdots, v_{max_n}\}$$
$$\textit{s.t.}\ v_{max_k} = max_{i\in\mathcal{L}}\ (G^{-1}e_k)^T\mathbf{i}, \mathcal{L} = \{\mathbf{i}|L\mathbf{i} \le I_m, \mathbf{i} \ge 0\} \quad (8)$$

And the prototype vectorless power grid verification framework can be described as follows:

Algorithm 1. Prototype Vectorless Power Grid Verification Framework

1. For $k = 1$ to n
2. Maximize $v_k = (G^{-1}e_k)^T\mathbf{i}$ s.t. $\mathbf{i} \in \mathcal{L}$
3 Let $v_{max_k} = max\ v_k$
4. End For
5. Find $v_{max} = max\ \{v_{max_1}, v_{max_2}, \cdots, v_{max_n}\}$

The general framework of the proposed approach which is based on the maximum voltage drop location estimation technique is shown in algorithm 2. In this framework, power grid nodes are checked in a group-by-group manner. We first try to pick out the possible "worst" power grid nodes in a certain group, and then perform accurate verification on these nodes.

In fact, the proposed verification framework is an approximate approach since the maximum voltage drop location estimation algorithm may make a wrong prediction. However, both of the theoretical analysis and experimental results have shown that if we can choose a good estimating function and select the nodes which will be analyzed in one group properly, the accuracy of the maximum voltage drop location estimation algorithm will be quite good. We can further improve the estimation accuracy by checking the power grid nodes which may have the largest k_0 voltage drops ($k_0 < k$) in one group based on the prediction made by the estimation algorithm.

If we use the upper bound defined by (7), the problem will become more difficult to solve. It seems that we must solve the element-wise maximization problem completely in order to get the upper bound of worst-case voltage drop vector. But we can combine the proposed approach with the sparse approximate inverse technique to overcome this difficulty. Let

$$V_a = emax_{\forall\mathbf{i}\in\mathcal{F}}(A^{-1}\mathbf{i}) \quad (9)$$

The framework described in Algorithm 2 can be used to make an estimation of the largest q elements in V_a with minor modifications. Sparse approximate inverse methods such as SPAI [3] can be used to find an approximation to $I + G^{-1}C/\Delta t$ which basically ignore the extremely small values in this matrix. So we can find out the node that may have the maximum voltage drop based on these results and then compute the exact value of the maximum voltage drop.

Algorithm 2. Vectorless Power Grid Verification Using Maximum Voltage Drop Location Estimation

Node grouping based on circuit partitioning

1. Divide the set of power grid nodes into k subsets: $N = N_1 \cup N_2 \cup \cdots \cup N_k$
2. Let $num = max\ \{|N_1|, |N_2|, \cdots, |N_k|\}$
3. For $j = 1$ to num
4. Select one node from each subset unless it is empty: $G_j = \{P_{j1} \in N_1, P_{j2} \in N_2, \cdots, P_{jk} \in N_k\}$
5. $N_1 = N_1 \setminus \{P_{j1}\}, \cdots, N_k = N_k \setminus \{P_{jk}\}$
6. End For

Verification procedure

7. For $j = 1$ to num

Maximum voltage drop location estimation

8. Maximize $f(\mathbf{i}) = f(v_{P_{j1}}, v_{P_{j2}}, \cdots, v_{P_{jk}})$ s.t. $\mathbf{i} \in \tilde{\mathcal{L}}$
9. Let $\mathbf{i}_j^* = argmax_{\mathbf{i}\in\tilde{\mathcal{L}}}\ f(\mathbf{i})$
10. Find

$$v_{P_{j^*}}(\mathbf{i}_j^*) = max\ \left\{v_{P_{j1}}(\mathbf{i}_j^*), v_{P_{j2}}(\mathbf{i}_j^*), \cdots, v_{P_{jk}}(\mathbf{i}_j^*)\right\}$$

Accurate verification

11. Maximize $v_{P_{j^*}} = \left(G^{-1}e_{P_{j^*}}\right)^T\mathbf{i}$ s.t. $\mathbf{i} \in \mathcal{L}$
12. Let $v_{max_j} = max\ v_{P_{j^*}}$
13. End For
14. Find $v_{max} = max\ \{v_{max_1}, v_{max_2}, \cdots, v_{max_{num}}\}$

B. Estimating Function

The construction of the objective function (line 8 in algorithm 2) used in the maximum voltage drop location estimation procedure is the most critical aspect in the proposed verification framework. The estimating function should be easy to optimize while the estimation accuracy should also be guaranteed.

First, consider the maximum function

$$g(\mathbf{i}) = max\ \{v_{P_{j1}}, v_{P_{j2}}, \cdots, v_{P_{jk}}\} \quad (10)$$

If we use $g(\mathbf{i})$ as the objective function for maximum voltage drop location estimation, the resulting maximization problem:

$$\textit{Maximize}\ g(\mathbf{i}) = max\ \{v_1, v_2, \cdots, v_n\} \quad \textit{s.t.}\ \mathbf{i} \in \mathcal{L} \quad (11)$$

is exactly equal to the problem defined by (8). The function

$$h(\mathbf{i}) = ln(e^{v_{P_{j1}}} + e^{v_{P_{j2}}} + \cdots + e^{v_{P_{jk}}}) \quad (12)$$

is a differentiable approximation to $g(\mathbf{i})$. In fact, $g(\mathbf{i})$ can be also interpreted as the infinity norm of the upper bound vector $\mathbf{v}_{max}$. So every function which is constructed based

on the general p-norm

$$r(\mathbf{i}) = \left(v_{P_{j1}}^p + v_{P_{j2}}^p + \cdots + v_{P_{jk}}^p\right)^{1/p} \ (p \geq 1) \quad (13)$$

can be used as an approximation to $g(i)$.

However, since $g(\mathbf{i})$ is a convex function, when it is used in the nonlinear programming which is usually formulated as a minimization problem, the objective function $-g(\mathbf{i})$ becomes a concave function. So the resulting optimization problem is very difficult to solve. Even if we just want to obtain an ε-optimal solution, the computation speed is still not fast enough. Other functions such as $h(\mathbf{i})$ and $r(\mathbf{i})$ $(p > 1)$ also suffer the similar disadvantage. Hence, we choose the function which can be interpreted as the 1-norm of the upper bound vector $\mathbf{v}_{max}$ as the estimating function:

$$f(\mathbf{i}) = v_{P_{j1}} + v_{P_{j2}} + \cdots + v_{P_{jk}} \quad (14)$$

The optimization of this linear function is quite easy. But $f(\mathbf{i})$ is not a very good approximation to $g(\mathbf{i})$ since the difference between the 1-norm and the infinity norm is relatively large. To ensure the estimation accuracy, we must take advantage of the locality effect of the power grid [3, 11].

A possible better choice is to use the weighted 1-norm:

$$f(\mathbf{i}) = w_1 v_{P_{j1}} + w_2 v_{P_{j2}} + \cdots + w_k v_{P_{jk}} \ (w_l > 0) \quad (15)$$

to handle the influence of current constraints in $\tilde{\mathcal{L}}$. For example, we can compute the number of conflicts between a certain node P_l and the other nodes in the same group and denote it by c_l. We can also compute the maximum distance d_l between P_l and the other nodes approximately by using the distance between the general parts they belong to (This will be introduced in the next section). So it appears to be a reasonable choice to set

$$w_l = 1 + 0.5\frac{c_l}{c_{max}} + 0.5\frac{d_l}{d_{max}} \quad (16)$$

where $c_{max} = max_{l \in G_j}\{c_l\}$ and $d_{max} = max_{l \in G_j}\{d_l\}$.

The analysis of the estimation accuracy can be established as follows. For an arbitrary node P_a on the power grid, let

$$\mathbf{i}_{P_a}^* = argmax_{\mathbf{i} \in \mathcal{L}} \, v_{P_a}(\mathbf{i}) \quad (17)$$

and decompose the vector into two non-overlapping parts:

$$\mathbf{i}_{P_a}^* = \mathbf{i}_{P_a}^1 + \mathbf{i}_{P_a}^2 \quad (18)$$

Then according to the locality effect of the power grid, we can assume that the voltage drop on this node is mainly caused by $\mathbf{i}_{P_a}^1$, i.e.,

$$v_{P_a}(\mathbf{i}_{P_a}^1) \geq (1 - \delta_1) v_{P_a}(\mathbf{i}_{P_a}^*) \ (\delta_1 > 0) \quad (19)$$

while $\mathbf{i}_{P_a}^1$ contains only a few nonzero elements. If the power grid nodes which are selected to be analyzed in the same group are well separated, we can ensure that all of the nonzero elements in $\mathbf{i}_j^1 = \mathbf{i}_{P_{j1}}^1 + \mathbf{i}_{P_{j2}}^1 + \cdots + \mathbf{i}_{P_{jk}}^1$ will also be contained in $\mathbf{i}_j^* = argmax_{\mathbf{i} \in \tilde{\mathcal{L}}} f(\mathbf{i})$ by making minor modifications to the original feasible region $\mathcal{L}$. Since the difference between $\tilde{\mathcal{L}}$ and $\mathcal{L}$ is not very large, we can make the assumption that for any node P_a in this group, the following inequality holds:

$$v_{P_a}(\mathbf{i}_j^*) \leq (1 + \delta_2) v_{P_a}(\mathbf{i}_{P_a}^*) \ (\delta_2 > 0) \quad (20)$$

Combing (19) and (20), we can get that

$$\mu v_{P_a}(\mathbf{i}_j^*) \leq v_{P_a}(\mathbf{i}_{P_a}^*) \leq \lambda v_{P_a}(\mathbf{i}_j^*) \quad (21)$$

where

$$\lambda = \frac{1}{1-\delta_1} \quad \text{and} \quad \mu = \frac{1}{1+\delta_2} \quad (22)$$

Now we can analyze the accuracy of the proposed algorithm under the assumption that the exact worst-case voltage drop $v_{P_a}^* = v_{P_a}(\mathbf{i}_{P_a}^*)$ at P_a can be treated as a uniformly distributed random variable. Suppose that we have already calculated the approximate values of the worst-case voltage drops at two grid nodes P_a and P_b by optimizing the objective function $f(\mathbf{i})$, and the result is $v_{P_a} > v_{P_b}$. So the maximum voltage drop location estimation algorithm will predict that $v_{P_a}^* > v_{P_b}^*$. The probability that we have made a right prediction is:

$$P = \begin{cases} 1 & , \ \mu v_{P_a} \geq \lambda v_{P_b} \\ 1 - \dfrac{\left(\lambda v_{P_b} - \mu v_{P_a}\right)^2}{\left(\lambda v_{P_a} - \mu v_{P_a}\right)\left(\lambda v_{P_b} - \mu v_{P_b}\right)} & , \ \mu v_{P_a} < \lambda v_{P_b} \end{cases} \quad (23)$$

The inequality (21) also provides a way to compute a conservative upper bound of the maximum voltage drop.

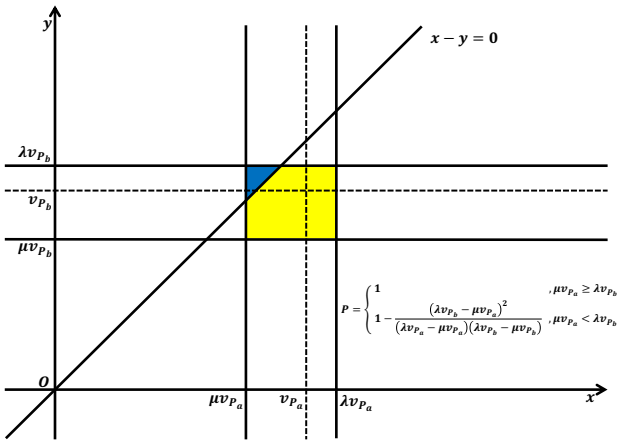

Fig. 1. Estimation accuracy analysis.

C. *Node Grouping Based on Circuit Partitioning*

From the analysis above, we can see that the main purpose of the node grouping procedure is to guarantee that all nodes in the same group are well separated. In order to achieve this goal, we first partition the power grid into several non-overlapping parts. Then each time we select one node from each part to generate a new group. Therefore, a good circuit partitioning algorithm is needed in the proposed verification framework.

There are many existing power grid partitioning algorithms. The partitioning approach introduced in [11] is a "shell"-based partitioning technique that specifically takes advantage of the locality effect of the power grid under C4 packaging. The disadvantage of this method is that it needs the detailed geometric information of the power grid. As a result, the partition strategy will become much more complicated when dealing with a 3-D irregular power grid. Alge-

braic circuit partitioning techniques are also been studied in many works [5, 12]. These methods try to decompose the power grid by adopting existing graph partitioning algorithms. The method used in [12] is in fact an algebraic $\mathcal{H}$-matrix splitting technique. In this paper, we use a similar technique which is introduced in [13] and make some simplification since the hierarchical property is not needed.

However, although these algebraic circuit partitioning techniques can handle the irregular structure of the power grid very well, they cannot deal with the impact of VDD pads. The basic idea of these methods can be interpreted as estimating the influence between any two nodes by computing the shortest path length connecting them in the resistance network. Hence, only the off-diagonal elements in the matrix are used while the information about the location of voltage sources is actually contained in the values of diagonal elements. This can be seen in Fig. 2. The lengths of shortest paths from P_0 to P_1, P_2 and P_3 can reflect the influence between each pair of nodes correctly. However, if there is a VDD pad nearby, this strategy will fail to give a right estimate.

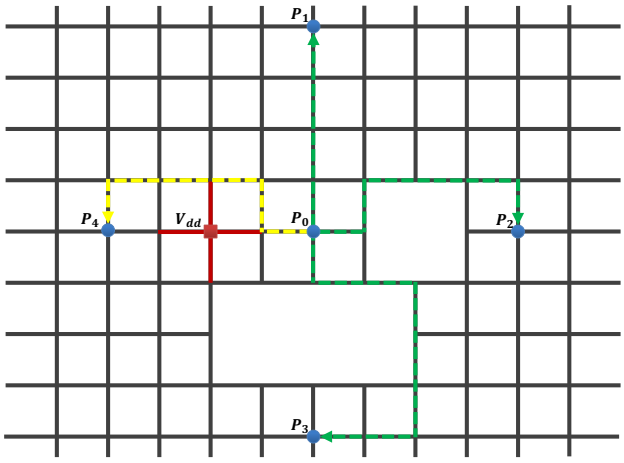

Fig. 2. The impact of VDD pads.

To overcome this difficulty, we propose a technique that takes the impact of VDD pads into consideration by changing the original values of the off-diagonal elements in the matrix. The modification is done in a level-by-level manner. The level of each node is determined by the breadth first search (BFS) algorithm. First, we pick out all the nodes which are connected to voltage sources and denote the set of these nodes by S_1. This can be done purely algebraically since the following inequality only holds at these nodes.

$$g_{ii} > \sum_{j \neq i} |g_{ij}| = g_{sum} \tag{24}$$

We change the value of g_{ij} for all these nodes synchronously.

$$\eta = e^{1-\frac{g_{ii}}{g_{sum}}}, \quad g_{ij}^* = \eta g_{ij}, \quad g_{ji}^* = \eta g_{ji} \tag{25}$$

Then the inequality (24) will also be satisfied at the nodes that are connected to the nodes in S_1. So the modification procedure can be performed at the next level. If an off-diagonal element has been modified, it will be marked and no longer changed a second time. The stopping criteria can be controlled by

$$\eta < \varepsilon_0 \quad \text{or} \quad Level > Level_{max} \tag{26}$$

D. Modification of Feasible Region

In order to ensure that the nonzero elements in the current vector $\mathbf{i}_j^1 = \mathbf{i}_{P_{j1}}^1 + \mathbf{i}_{P_{j2}}^1 + \cdots + \mathbf{i}_{P_{jk}}^1$ will also be contained in $\mathbf{i}_j^* = argmax_{\mathbf{i} \in \mathcal{L}} f(\mathbf{i})$, we may need to make some small modifications to the original feasible region $\mathcal{L}$. So it is need to find the local support region $supp(P_a)$ of a certain power grid node P_a, which is in fact an approximation to the set of nonzero elements in the vector $\mathbf{i}_{P_a}^1$.

If we are dealing with the upper bound defined by (7), since a sparse approximation to $I + G^{-1}C/\Delta t$ will be computed, we can use this information to estimate the major elements in the inverse of $A = G + C/\Delta t$ and find the local support region for each node. If we only consider the upper bound defined by (6), a method which requires much less computational cost can be used. We can adopt the Dijkstra's algorithm to find the nearest n_0 grid nodes to P_a in the modified resistance network which has been used in the power grid partitioning procedure and get the local support region of P_a. Notice that although a larger local support region can guarantee a smaller δ_1, it may also cause conflict to the global current constraints, which will result in a larger δ_2. Hence, we restrict the size of each local support region by setting the value of n_0 to be about 25~41 and checking that there is no singular local support region that can cause conflict to any global current constraint.

After all the local support regions of the power grid nodes in one group have been found, we begin to modify the original feasible region $\mathcal{L}$. First, we add equality constraints to set every current source in these local support regions to its maximum allowable value. And then we check the original global current constraints and relax the ones which cannot be satisfied.

E. Complexity Analysis

In terms of complexity, since the node grouping procedure based on circuit partitioning can be performed in almost linear complexity, i.e., $O(n\log^{\alpha} n)$ with moderate parameter α [12] and needs to be done only once, the main factors that affect the total runtime are still the linear system solution and the linear programming solution in the for-loop. Verifying a single node on the power grid needs one linear system solution and one linear programming solution in the original verification framework. And we denote the runtime by T_e. The maximum voltage drop location estimation procedure require to solve one linear system to obtain the objective function $f(\mathbf{i})$, to solve one linear programming, and to solver another linear system to get the estimation result. So it is known that $2T_e < T_g < 3T_e$, where T_g is the runtime for verifying a group of nodes in the proposed framework. Hence, we can achieve about $\frac{n}{3num} \approx \frac{k}{3}$ times of speedups over the original method, in which num is the number of node groups and k is the number of partitions of the power grid.

IV. EXPERIMENTAL RESULTS

The proposed maximum voltage drop location estimation based vectorless power grid verification framework is implemented in C++. We use Cholmod [14] to solve the linear equations and lp_solve 5.5 [15] to solve the involved linear programming problems. For comparison, we also implement the original vectorless power grid verification framework based on Algorithm 1. All these experiments are performed on a 64-bit Linux machine with 2.33GHz Intel Xeon E5345 processor and 8GB RAM. The test cases are generated based on the power grids used in [5]. These power grids are mainly small and medium sized 3-D regular grids. In order to verify the accuracy of the maximum voltage drop location estimation method under different circumstances, we also generate several different types of test cases. The parameters of the test cases are shown in Table I.

TABLE I. TESTCASE PARAMETERS

Power Grid	Type	#Nodes	#VDD Pads	#Global Constraints
PG1	2-D irregular	4082	9	6
PG2	3-D regular	5875	9	10
PG3	2-D irregular	9964	16	10
PG4	3-D irregular	11706	18	10
PG5	3-D regular	22939	25	10
PG6	3-D irregular	35568	36	12

Experimental results of the entire framework are shown in Table II and Fig. 3. The function $\tilde{f}(\mathbf{i})$ in (15) is used as the estimating function for maximum voltage drop location estimation. In terms of verification accuracy, since accurate verifications are performed for all the nodes selected from each group, we can get a precise result of the worst voltage drop across the entire grid if the estimation algorithm can pick out the real "worst" node from a certain group. Even if the estimation algorithm makes several wrong predictions, the whole framework is still able to find a power grid node which has a relatively large worst-case voltage drop. In terms of runtime, since we do not implement any acceleration technique for the linear programming problem, the runtime cannot be compared with the results in [5] directly. From the experimental results we can see that the modified vectorless power grid verification framework can achieve about 15X speedups over the original method, which may be further improved on lager power grids according to the complexity analysis made above.

TABLE II. EXPERIMENTAL RESULTS

Test Case	#Partitions	Runtime			Error (mV)
		Original	Modified	Speedup	
PG1	16	122.46 s	21.16 s	5.79	0.17
PG2	16	293.75 s	48.63 s	6.04	0
PG3	25	996.41 s	105.43 s	9.45	7.53
PG4	32	25.36 m	122.76 s	12.40	0
PG5	36	1.72 h	424.35 s	14.60	0
PG6	36	5.14 h	20.66 m	14.92	2.81

V. CONCLUSIONS

In this paper, we present a modified vectorless power grid verification framework using a maximum voltage drop location estimation technique. By picking out the nodes which may have the maximum worst-case voltage drop in advance, the whole verification cost is significantly reduced. Experimental results have confirmed that the proposed estimation approach is accuracy and efficient for practical use. The modified resistance network which is introduced for the node grouping procedure of the estimation algorithm can be also used on other occasions such as the preconditioner construction for iterative linear solvers.

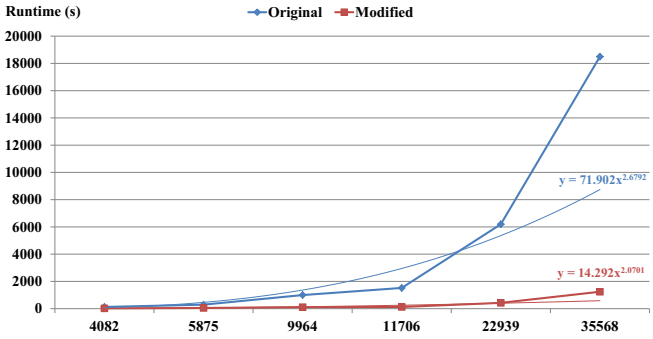

Fig. 3. Runtime comparison.

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